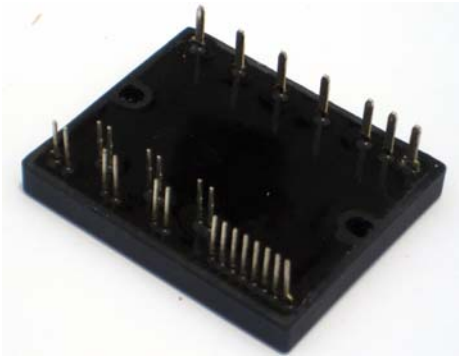
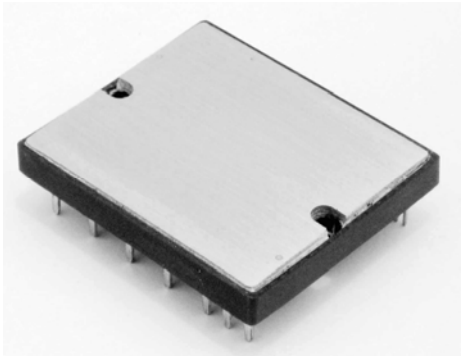
2010-05-17

STARPOWER ID- IPM Application Note





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Chapter 1 Starpower IPM Product Outlines

1.1 Introductions

Inverter technology brings obviously advantages like: energy efficient and quiet-running compare to the conventional motor drives technology. With the advantages of compactness, built-in control, and lower overall-cost modules requirements are increasing for low-power motor control applications. Starpower's ID series IPM is provided with compact, high-functionality, and high efficiency to meet these needs.

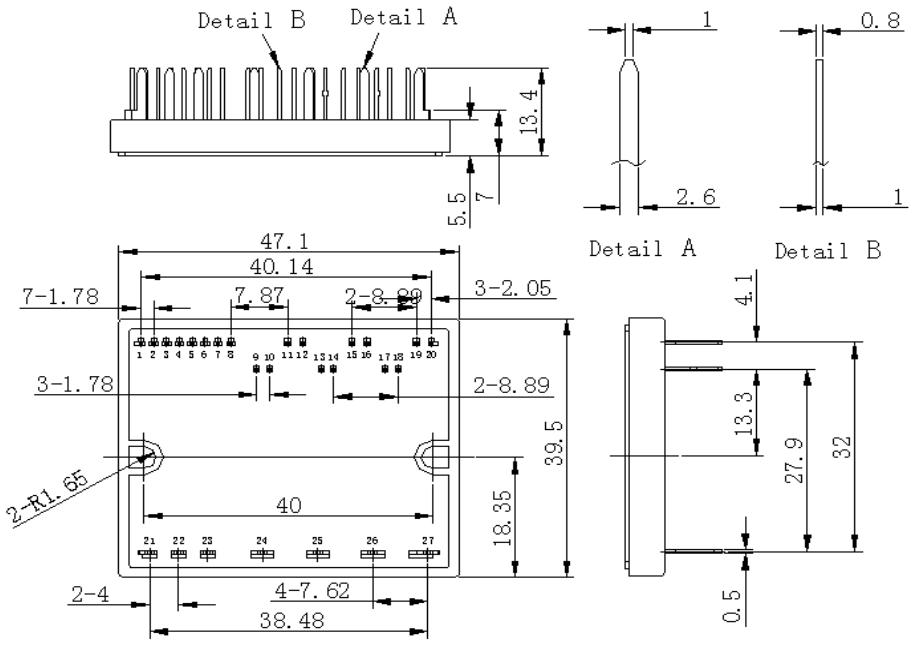
ID series IPM is an attractive choice which alternative to conventional discrete solution for low-power motor drives, specifically for appliances such as air conditioning, washing machines. ID series IPM combines optimized driver and protection circuit which matched to the IGBT's switching characteristics. ID series IPM is also provided with highly effective short-circuit detection and protection functions through the use of real time current sensing technique together with under-voltage protection function to prevent over heat condition when driving voltage is not working normally.

This application note shows the details of ID series IPM. The designer could easily understand and learn how to adopt the parts to his system design by aid of the quick study of the application note.

1.2 Starpower ID-IPM Outlines and Series

Figure 1-1. Outline of ID-IPM (ID20FT06A1S)

1.2.1 Drawing



TERMINAL CODE

1 VCC	15 VB(V)
2 COM	16 VS(U)
3 IN(UL)	17 IN(WH)
4 IN(VL)	18 VCC
5 IN(WL)	19 VB(W)
6 VFO	20 VS(W)
7 CFOD	21 NU
8 CSC	22 NV
9 IN(UH)	23 NW
10 VCC	24 U
11 VB(U)	25 V
12 VS(U)	26 W
13 IN(VH)	27 P
14 VCC	

Figure 1-2. Package Outlines

1.2.2 Ordering Information

ID 20 F T 06 A1 S

(1) (2) (3) (4) (5) (6) (7)

(1) Device: Intelligent Power Module
(2) Current Rating: 20=20A
(3) Circuit Configuration: F=Three Phase, P=Seven Pack
(4) Chip Characteristics: L=NPT Low Loss, T=Trench Low Loss
(5) Voltage Rating: 06=600V, 12=1200V
(6) Package Style
(7) Options

1.2.3 Starpower ID-IPM Series

Table 1-1. Starpower ID-IPM Series and General Applications

Part Number	Ratings	Motor Ratings(*)	PWM Frequency(Typ.)	Remark
ID10FT06A1S	600V/10A	0.5 KW/220Vac	15kHz	V_{iso} = AC 2500V_{rms} (Sinusoidal 1min)
ID15FT06A1S	600V/15A	0.75 KW/220Vac	15kHz	
ID20FT06A1S	600V/20A	1.5 KW/220Vac	15kHz	
ID30FT06A1S	600V/30A	2.2 KW/220Vac	15kHz	

1.3 Home appliances & Industrial application

Motor drive for household electric appliances: air conditioners, washing machines, refrigerators, low power industrial applications such as treadmill and general purpose inverter as well. IPM is the best choice for the low power motor drivers.

Figure 1-3. Home and industrial application areas

1.4 Internal circuit and Features

1.4.1 Internal Block Diagram

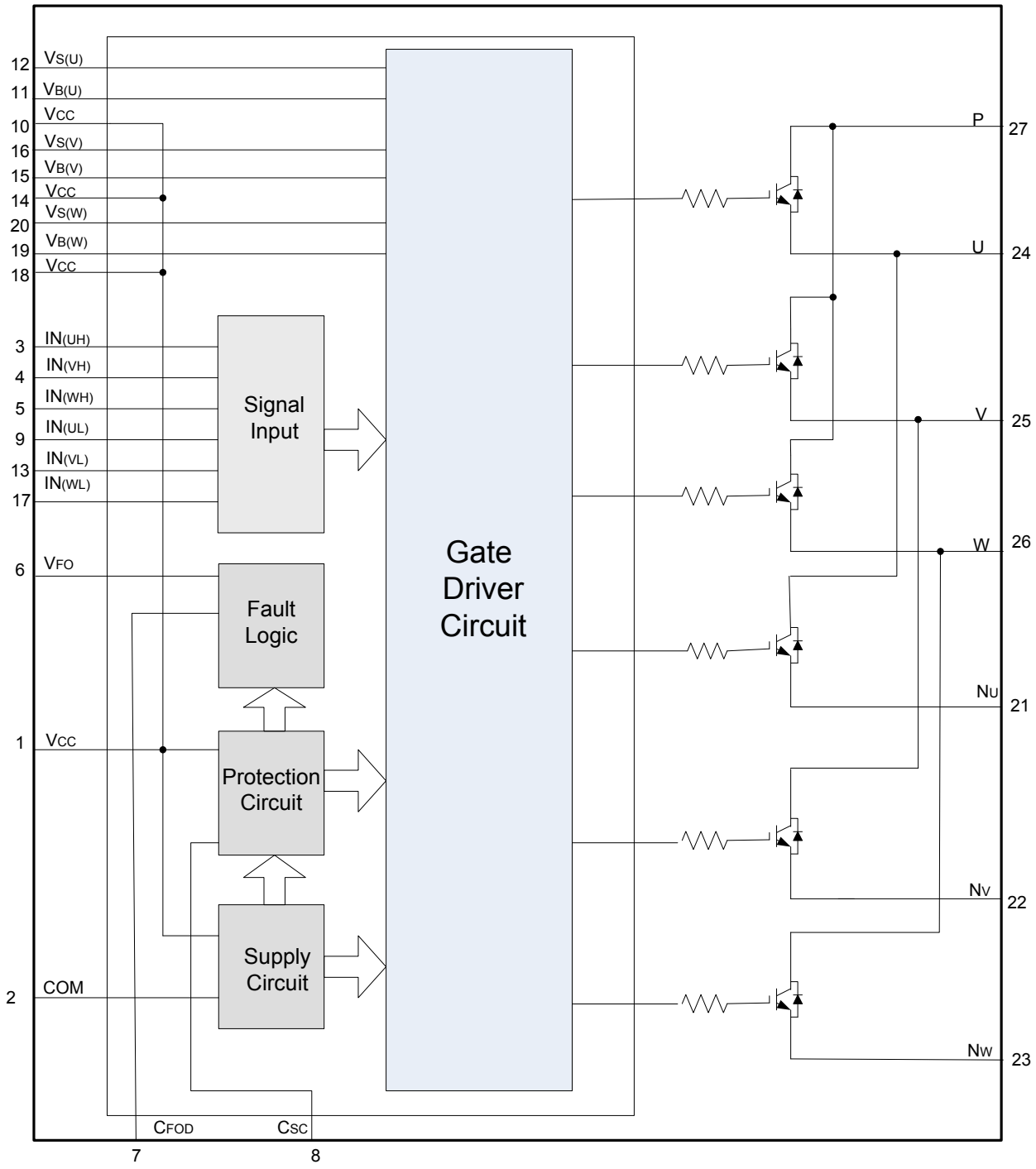


Figure1-4 Internal Block Diagram of Starpower ID IPM

1.4.2 Features and Functions

Features

- UL Certified (UL 1557).
- Low power dissipation and excellent thermal package design.
- Low temperature coefficient effect both for driver and IGBT.
- Divided negative dc-link terminals for inverter current sharing application.
- Matched propagation delay for all channels.
- Lead-Free packaging and RoHS compatible.
- Provided a fault signal (V_{FO} pin) and shut-off internal IGBT when OC/SC and under-voltage event occur.

Chapter 2 Electrical Characteristics

2.1 Description of the Input and Output Pins

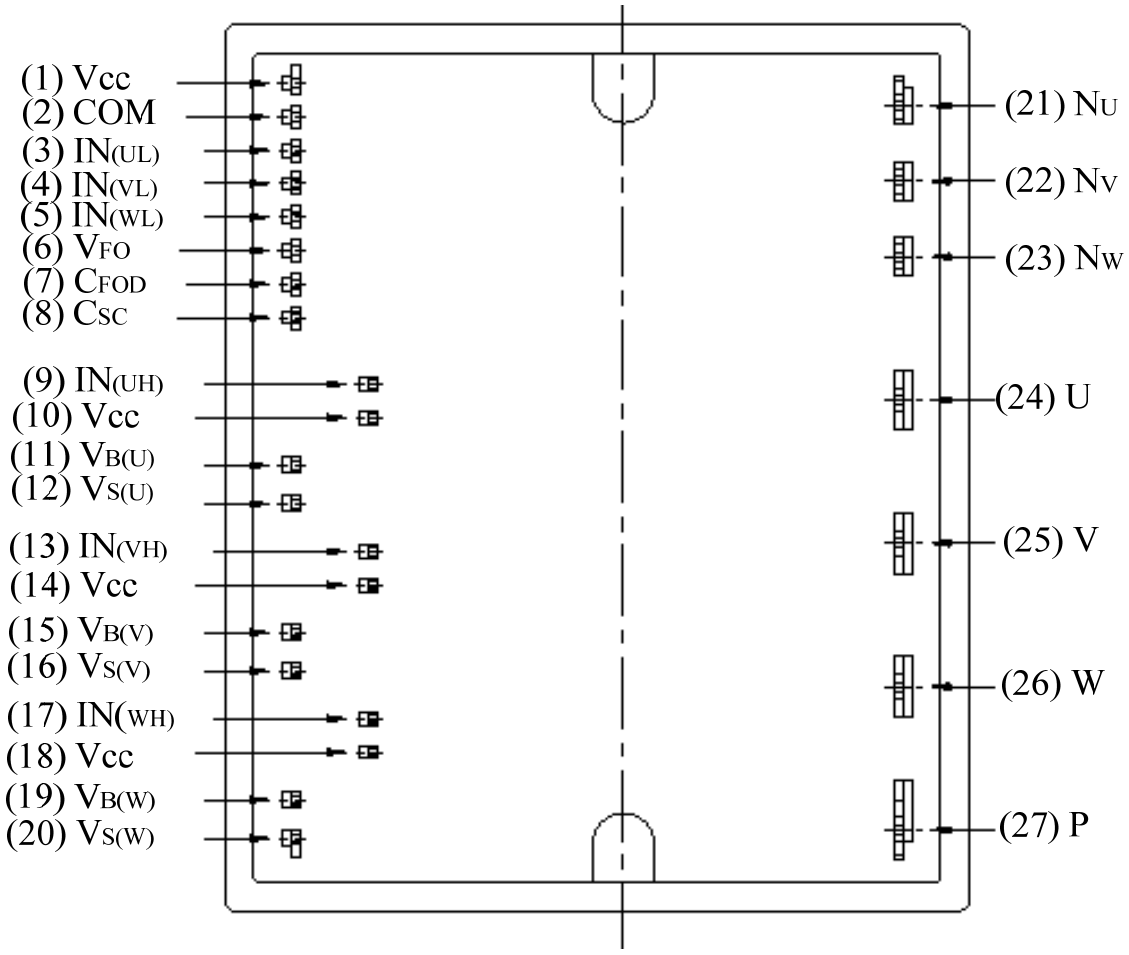


Figure 2-1. Pin Definition of ID IPM (ID20FT06A1S)

No.	Symbol	Pin Description
1	V_{CC}	Supply Voltage Terminal for Driver IC
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-side U Phase
4	$IN_{(VL)}$	Signal Input for Low-side V Phase
5	$IN_{(WL)}$	Signal Input for Low-side W Phase
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault Output Duration Time Selection
8	C_{SC}	Capacitor (Low-pass Filter) for Short-Current Detection Input
9	$IN_{(UH)}$	Signal Input for High-side U Phase
10	V_{CC}	Supply Voltage for Driver IC
11	$V_{B(U)}$	High - side Bias Voltage for U Phase IGBT Driving
12	$V_{S(U)}$	High - side Bias Voltage Ground for U Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High-side V Phase
14	V_{CC}	Supply Voltage for Driver IC
15	$V_{B(V)}$	High - side Bias Voltage for V Phase IGBT Driving
16	$V_{S(V)}$	High - side Bias Voltage Ground for V Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High-side W Phase
18	V_{CC}	Supply Voltage for Driver IC
19	$V_{B(W)}$	High - side Bias Voltage for W Phase IGBT Driving
20	$V_{S(W)}$	High - side Bias Voltage Ground for W Phase IGBT Driving
21	N_U	Negative DC-Link Input for U Phase
22	N_V	Negative DC-Link Input for V Phase
23	N_W	Negative DC-Link Input Terminal for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC – Link Input

2.1.2 Pin Descrition

Supply source of the ID- IPM

Pin symbol：V_{CC}

- V_{CC} is internal connected together.
- It is necessary to mount (as possible as close to these pins) a capacitor of favorable frequency to prevent malfunction caused by the unstable operation.
- To prevent damage the internal driver IC. So, it is necessary to keep the operation supply voltage below the maximum specified values.

Grounding port

Pin symbol：COM

- This is the driver ground for the internal driver IC.
- Main loop current of the power circuit loop should not be allowed to flow through these terminals to avoid noise influences.

Short-circuit trip voltage sensing port

Pin symbol：C_{SC}

- The designer need to insert the current sensing resistor between this terminal and GND to detect OC/SC situations.
- The port may recognize the noise as the real input, so the designer need to add a suitable RC filter to reduce the noise level but don't delay the actual signal.

Fault pulse output time setting port

Pin symbol：C_{FOD}

- This port is used for setting the fault pulse output time.
- In order to set the fault pulse output time, the designer may need to add an external capacitor between this port and ground (reference).

External RC network input used to define FAULT CLEAR delay, TFO, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-collector high-impedance.

Fault output port

Pin symbol：V_{FO}

- This terminal will be pulled down to low level in case abnormal condition SC/OC and under-voltage lockout protection is active.
- Because the port is a open collector topology. The signal fit to the FO port is recommended to pulled up to the 5V power supply with approximately 4.7KΩ resistance.

Control input port

Pin symbol：$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$

- Active logic corresponding to the state of the IGBT.
- These pins are input port which is used to detect the controlling pattern to active the IGBT for switching.
- To put RC filter in front of the input port is recommended.
- In order to eliminate the noise when the signal level is changing its state, the trace from controller to the port is recommended as short as possible.

High-side drive supply port / High-side drive supply reference port

Pin symbol：$V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$

- The bootstrap circuit scheme is needed for driving high side IGBTs by using single supply source.
- B(x)-S(x) means the input voltage terminal for high-side IGBTs.
- It is necessary to mount(as possible as close to these pins) a capacitor of favorable frequency to prevent malfunction caused by the unstable operation.

Inverter positive power supply port

Pin symbol：P

- DC-Link positive terminal connected to the collectors of the high-side IGBTs internally.
- Effectively to add a good frequency characteristic capacitor to reduce the voltage spike result in persist inductance of the trace or wiring. And the smoothing capacitor is recommended to put as close to the P and N.

Inverter GND port

Pin symbol：N_U,N_V,N_W

- DC-Link negative terminal connected to the emitters of the low-side IGBTs internally.
- N_U :Negative DC-Link Input for U Phase.
- Nv :Negative DC-Link Input for V Phase.
- Nw :Negative DC-Link Input for W Phase.

Inverter power output port

Pin symbol：U, V, W

- Inverter output port which is used to connect to three phase load, ex induction motor or DC Brush less motor…etc.
- Each terminal is internally connected to the intermediate point of the corresponding IGBT half bridge arm.

2.2 Static Characteristics

Table 2-2. Characteristics of ID- IPM (ID20FT06A1S)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Collector-emitter breakdown voltage	V_{CES}	V_{SC} =5V, I_C=500μA	600	--	--	V
Collector-emitter saturation voltage	$V_{CE\ (sat)}$	V_{CC} =15V, V_{SC}=0V, I_C=20A, T_C =25℃	--	--	2.3	V
FWD forward voltage drop	V_F	V_{SC} =5V, -I_C=20A, T_C =25℃	--	--	2.1	V
Collector-Emitter cut-off current	Ices	V_{SC} =5V, V_{CE} =600V	--	--	100	μA

Table 2-3. Characteristics of ID- IPM control part (ID20FT06A1S)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
$IN_{(UH、VH、WH)}$, $IN_{(UL、VL、WL)}$ ON threshold voltage	$V_{IN\ (on)}$		2.5	--	--	V
$IN_{(UH、VH、WH)}$,$IN_{(UL、VL、WL)}$ OFF threshold voltage	$V_{IN(off)}$		--	--	0.8	V
$IN_{(UH\ 、\ VH\ 、\ WH)}$ input bias current	$I_{IN(UH、VH、WH)(HI)}$	$V_{IN(UH、VH、WH)}$ = 5V	-	-	200	μA
	$I_{IN(UH、VH、WH)\ (LO)}$	$V_{IN(UH、VH、WH)}$ = 0V	-1	-	-	
$IN_{(UL、VL、WL)}$ input bias current	$I_{IN(UL、VL、WL)\ (HI)}$	$V_{IN(UL、VL、WL)}$ = 5V	-	-	200	μA
	$I_{IN(UL、VL、WL)\ (LO)}$	$V_{IN(UL、VL、WL)}$ = 0V	-1	-	-	
Driver IC supply voltage	V_{CC}		11.5	15.0	20.0	V
P - side floating supply voltage	$V_{B(U)S(U),\ B(V)S(V),\ B(W)S(W)}$		11.5	15.0	20.0	V
V_{CC} terminal input current	I_C		-	1.6	2.3	mA
Fault output voltage	V_{FOH}	V_{SC} =0V	4.9	-	-	V
	V_{FOL}	V_{SC}=1V	-	-	200	mV
Short circuit trip level	$V_{SC(ref)}$	V_{CC} =15V, T_j = 25℃	0.45	0.50	0.55	V
Fault output pulse width	t_{FOD}	$C_{F\ O\ D}$= 33nF	-	1.8	-	ms
Supply circuit under voltage protection	UV_{CCD}	Trip level	8.6	9.4	10.2	V
	U_{VCCR}	Detection level	9.6	10.4	11.2	V
	UVH	Hysteresis	-	1.0	-	V
$IN_{(UL、VL、WL)}$ Input filter time	$t_{IN,FIL}$	VIN = 0 & 5V	100	200	-	ns

2.3 Dynamic Characteristics

Table 2-4. Characteristics of ID- IPM (used ID20FT06A1S as the example)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Switching times	T_{on}	V_{CE}=300V, V_{CC} =15V, I_C=20A, $V_{IN(UH)}$ = $V_{IN(VH)}$ =$V_{IN(WH)}$= 0V→5V, T_C =25℃	--	1.08	--	μs
	T_r		--	0.20	--	
	Tc(on)		--	0.32	--	
	T_{off}		--	0.98	--	
	T_f		--	0.06	--	
	Tc(off)		--	0.50	--	
	Trr		--	0.13	--	

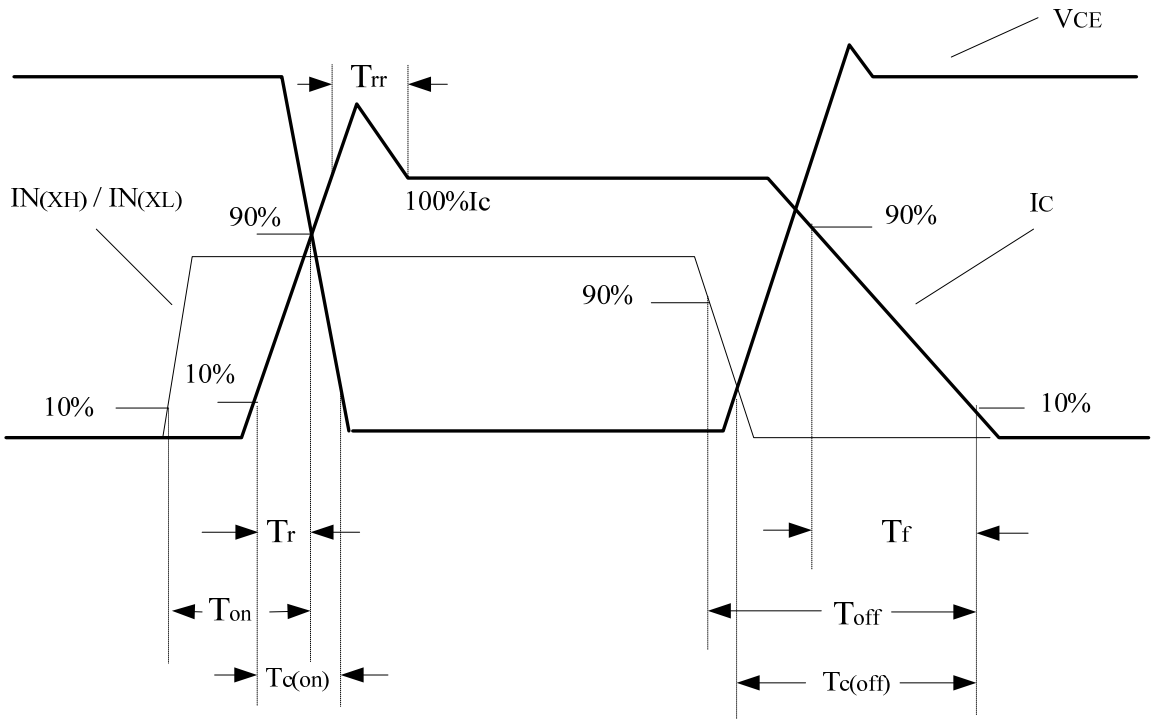


Figure 2-2. Definition of Switching Time

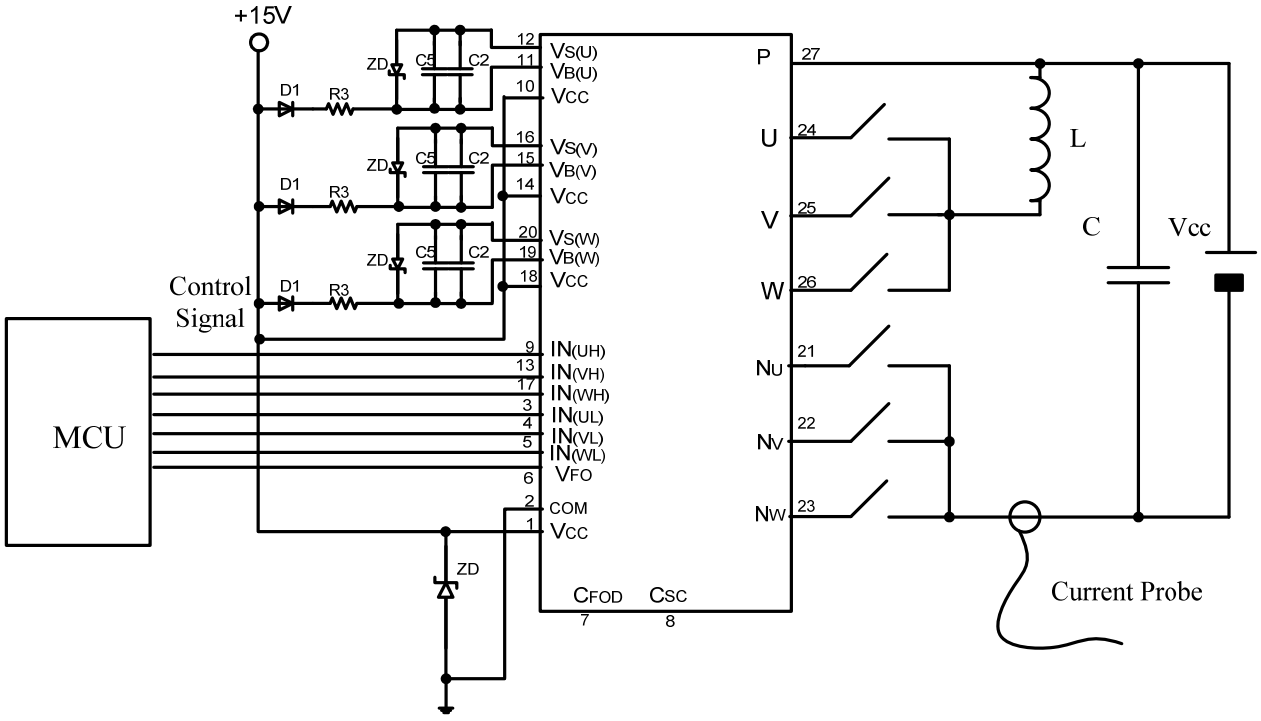


Figure 2-3. Evaluation Circuit Diagram (Inductive Load)

Note：V_{BS1}= V_{BS2}= V_{BS3}=Vcc=15V

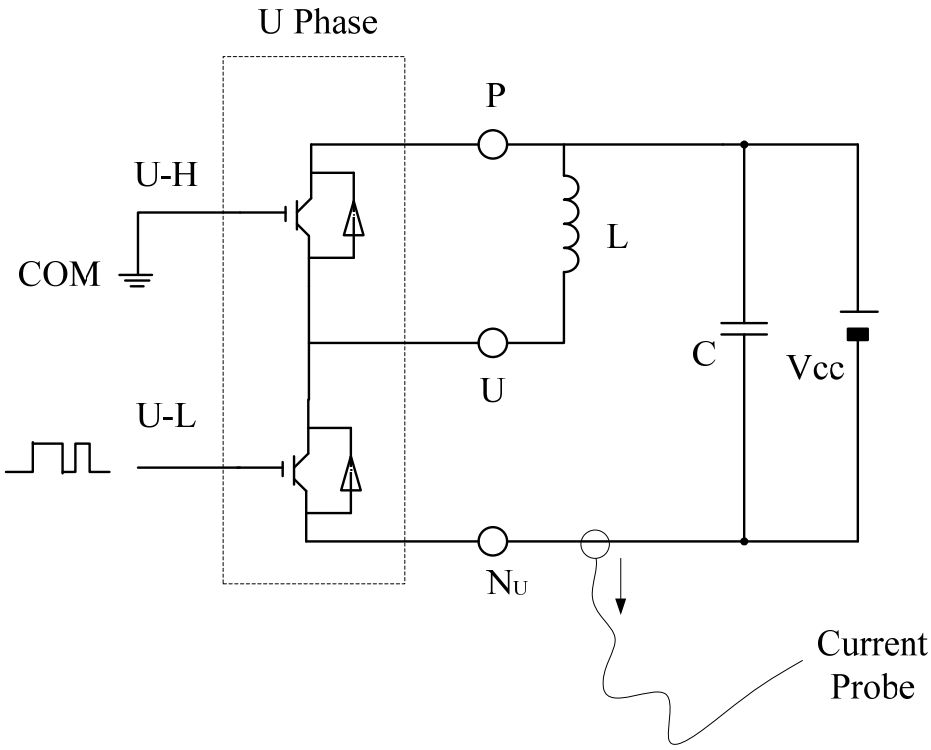


Figure 2-4. Test Circuit of Dynamic Parameter

Switching Characteristics

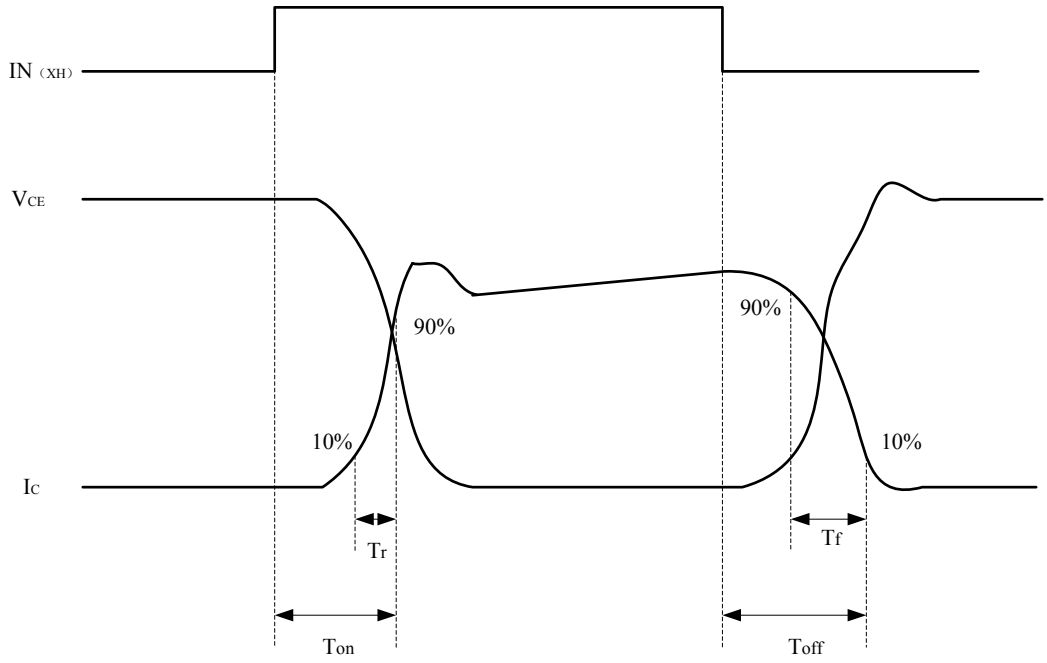
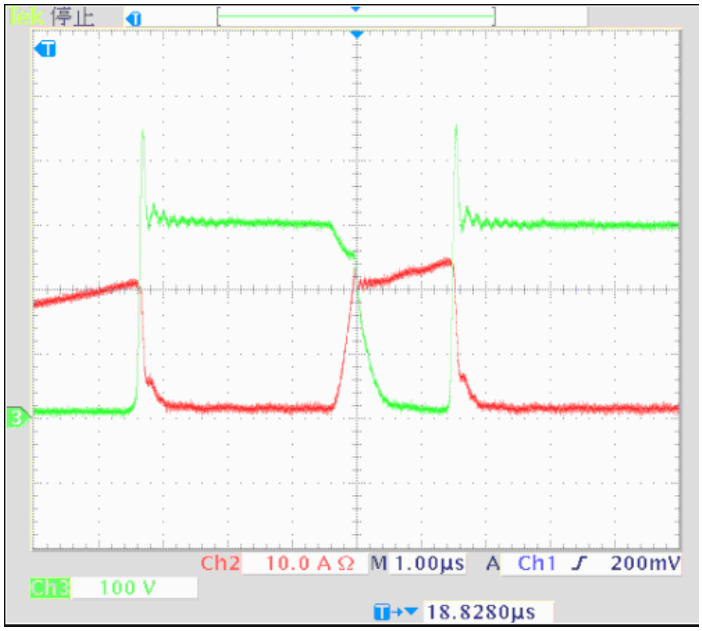


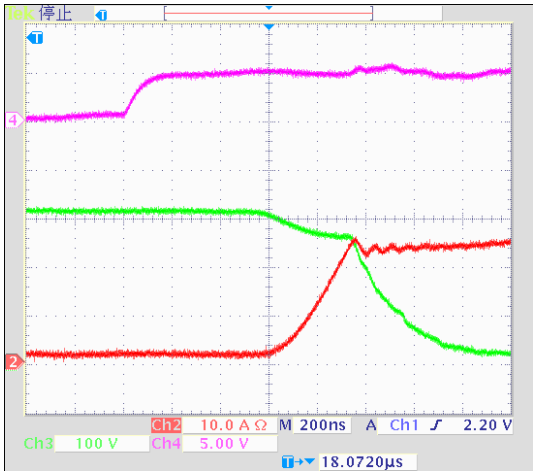
Figure 2-5. Switching Time Definition

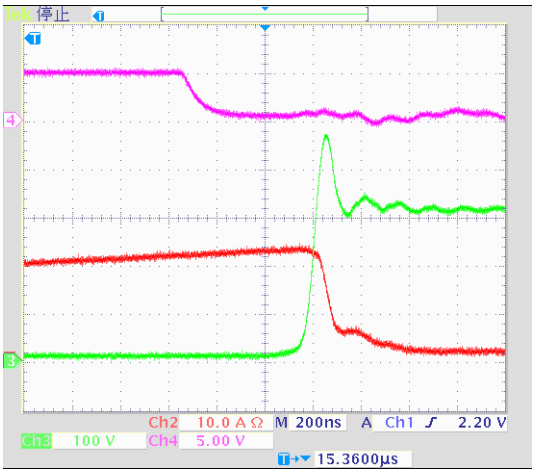
Part NO.：ID20FT06A1S

Test Conditions：V_{DC} = 300V, V_{CC} = 15V, I_C = 20A, Vin = 0V→5V, T_C = 25℃, Inductive Load Circuit

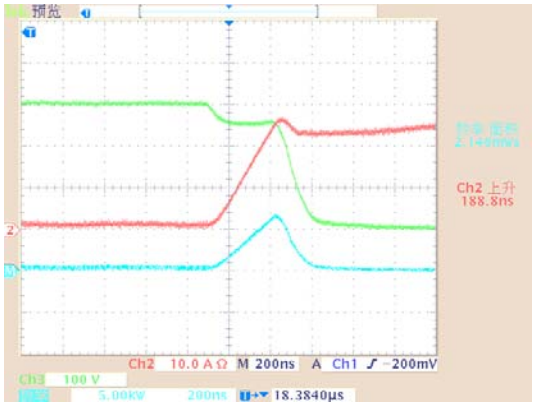
Ch2: I_C
Ch3: V_{CE}

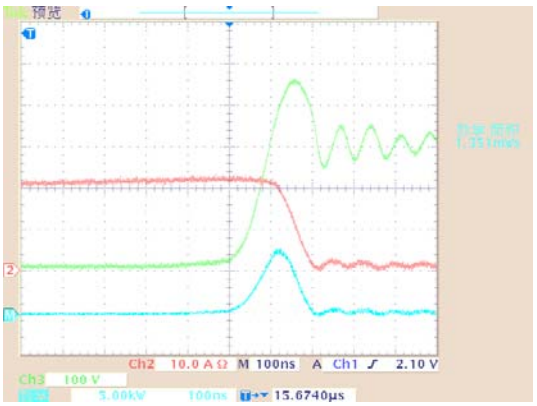






Ch2: I_C
Ch3: V_{CE}
Ch4: $IN_{(UH)}$





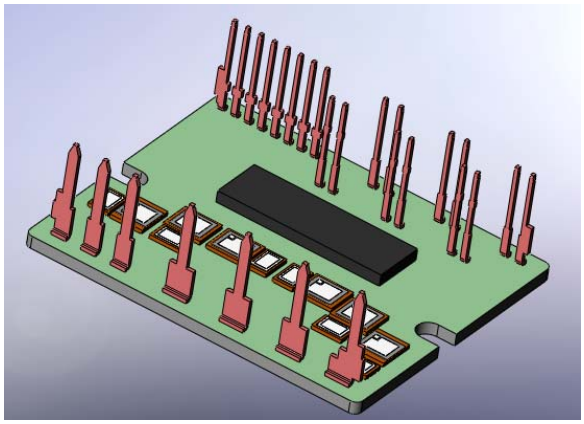
Ch2: I_C
Ch3: V_{CE}
M: Switching Loss

Figure 2-6. Switching Waveform of ID- IPM (Used ID20FT06A1S class) (Typ.)

Chapter 3 Packaging and Installation Guide

3.1 Package

3.1.1 Internal Structure Overview



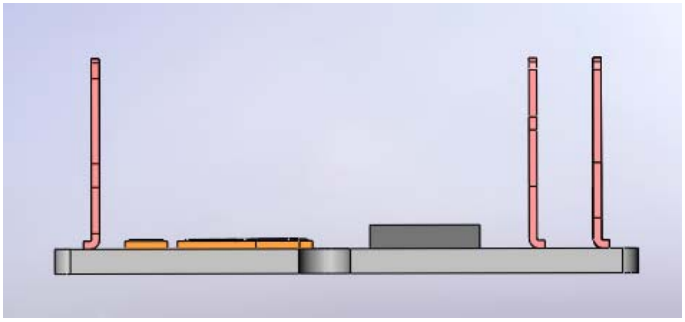


Figure 3-1. ID IPM Internal Structure

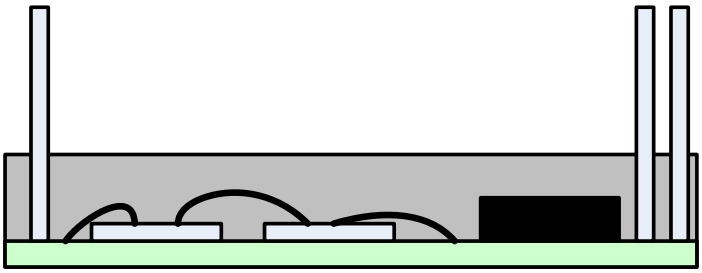


Figure 3-2. ID-IPM Package Cross Section

3.1.2 Driving and Protection Functions

Driving logic

- When the logic level of $IN_{(xH)}$ or $IN_{(xL)}$ is in high state then its corresponding IGBT will be “ON”. And when $IN_{(xH)}$ or $IN_{(xL)}$ is in low state then its corresponding IGBT will be “OFF”.
- Under-Voltage protection: if the input level of $V_{IN(xH)\ \&\ IN(xL)}$ is higher than $V_{th(on)}$ then IPM will work normally, If the input level of $V_{IN(xH)\ \&\ IN(XL)}$ is lower than $V_{th(off)}$, then IPM will shut-off its output.

Short circuit protection

- Usually the designer will use external shunt resistance to detect the injection DC-Link current to protect the load. When the current exceeds a preset SC trip level, it is judged as a short circuit state, and IPM will shut off its output immediately.
- Once the current is over the current limitation passing through the external shunt resistance. A fault pulse signal will output and the pulse duration will be determined by the capacitance of the capacitor connected between C_{FOD} and COM. After it is being outputted continuously for a certain period of time (depends on the capacitor), fault condition will be reset when the next input signal reaches the normal level.

Control supply circuit under voltage protection

- The protection is used to make sure the control supply voltage for high/low-side IGBT driving. Input signals to the high/low-side IGBTs are locked if the voltage falls below the trigger level for a given period of time.
- Only when the voltage exceeds the reset level of under-voltage protection, under-voltage protection won't be reset.
- Under-voltage protection fault pulse signal output period is determined by the capacitance of the external capacitor that is connected between C_{FOD} pin and COM pin. After fault signal is being outputted for a certain period of time, and the time is depends on the capacitor and the voltage level. The fault resetting takes place at the next input signal if the control supply voltage is over the reset level.

3.2 Installation Guide

3.2.1 Heat Sink Mounting

The following precautions should be observed to maximize the effect of the heat sink and minimize device stress, when mounting an ID- IPM on a heat sink. When apply silicon grease between the ID- IPM and the heat sink to reduce the contact thermal resistance. Be sure to apply the coating thinly and evenly, do not use too much. A uniform layer of silicon grease (100 ~ 200um thickness) should be applied in this situation. Fig. 3-3 shows the recommended silicon grease thickness.

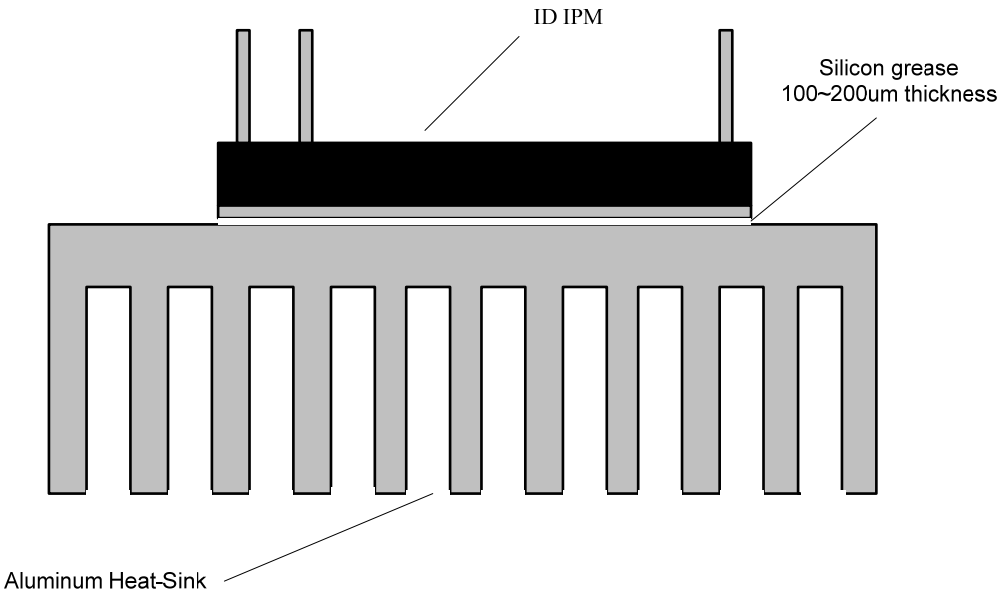


Figure 3-3. Recommended Silicon Grease Thickness

When attaching a heat-sink to an ID- IPM. Make sure not to apply excessive force to the device for assembly. Drill holes for screws in the heat sink exactly as specified. Smooth the surface by removing burrs and protrusions of indentations. Do not touch the heat-sink when IPM is operation to avoid sustaining a burn injury. Table 2-2 can provide the designer the guideline. Heat sink flatness is prescribed as seen in Figure 2-4.

Table 3-1. Mounting Torque and Heat Sink Flatness Specifications

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw：M3	Recommended 0.65 N•m	0.60	0.65	0.70	N•m
Heat-sink flatness		--	-50	-	0	μm

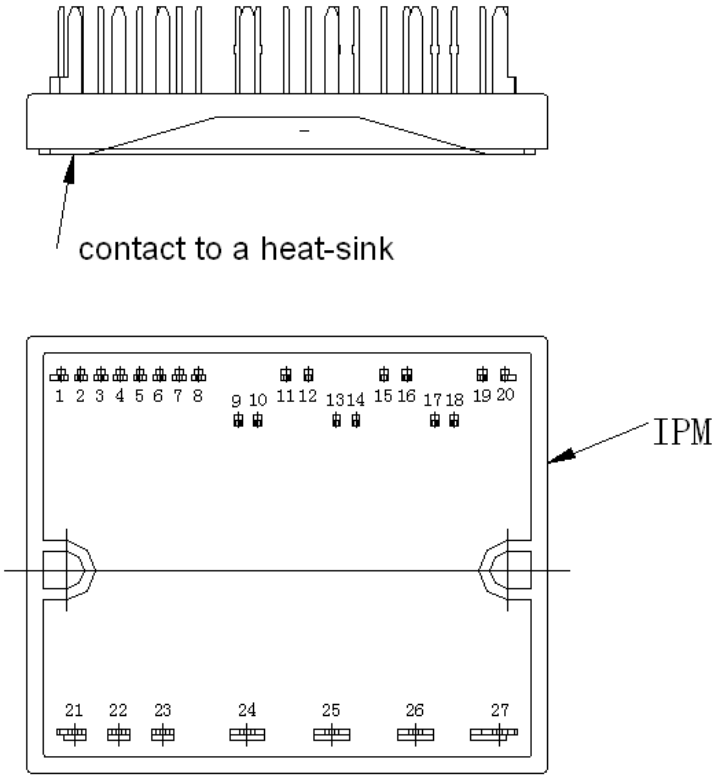


Figure 3-4. Measurement Point of Heat-sink Flatness

3.2.2 Screw Tightening Torque

Do not exceed the specified fastening torque. Over tightening the screws may cause molding compound crack and bolts with heat-fin destruction. Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance. The tightening torques in table 2-2 is recommended for obtaining the proper contact thermal resistance and avoiding the application of excessive stress to the device. Avoid stress due to

tightening on one side only. Figure 2-5 shows the recommended fastening order for mounting screws. In the first use screwdriver temporary fastening screws, then use screwdriver permanent fastening. Note that uneven mounting can cause the ID-IPM housing and molding compound to be damaged.

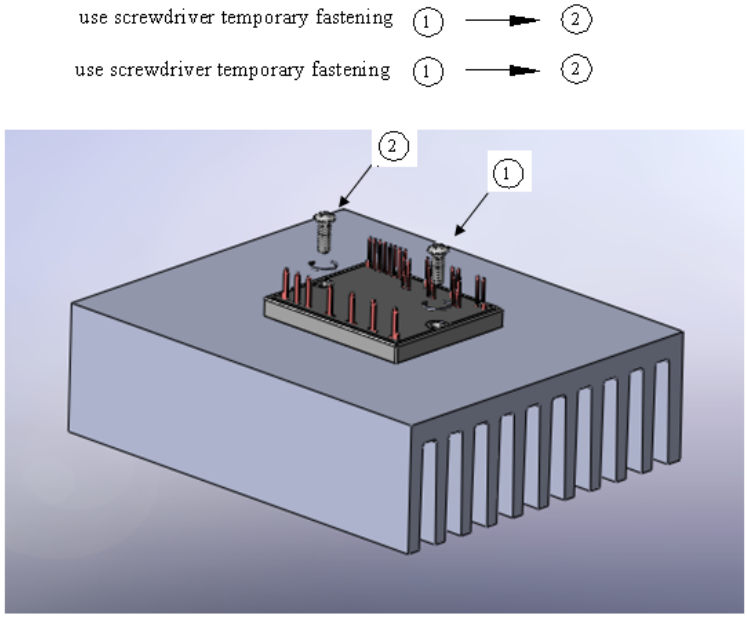


Figure 3-5. Recommended Fastening Order of Mounting Screws

The heat sink flatness (warp/concavity and convexity) on the module installation surface (refer to Figure 2-6), please follow the guidelines below in order to get effective heat-radiation when you want to enlarge the heat area.

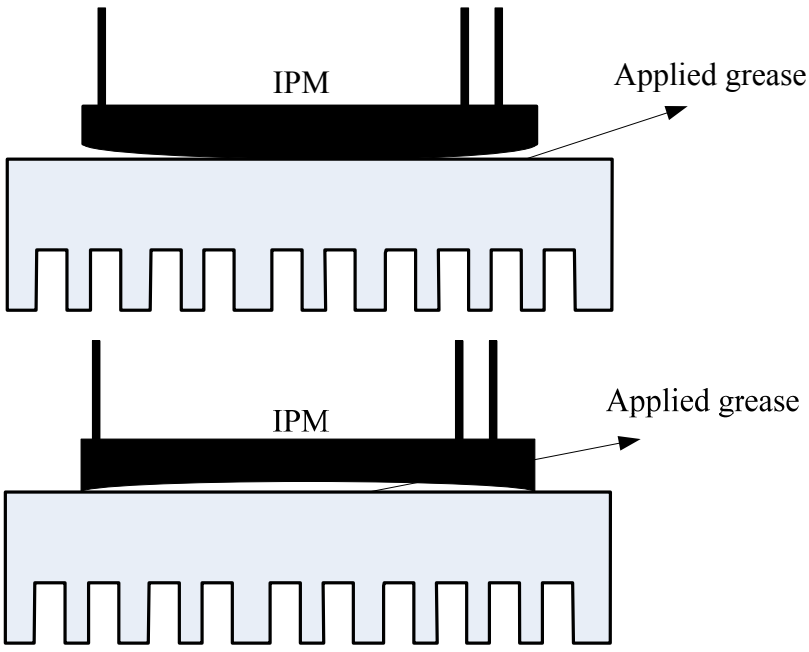


Figure 3-6. Heat Sink Flatness Specification

It will get better 100μm ~ 200μm of thermally-conductive grease over the contact surface between a module and a heat sink. It is also useful for preventing the contact surface from being corroded. Further, use a grease type of stable quality within the operating temperature range and have long endurance. Use a torque wrench to fasten up to the specified recommended torque. Exceeding the max data, torque limit might cause the modules to be damaged or to be degraded as the above-mentioned fastening with uneven stress. Foreign matter onto the contact surface between a module and a heat sink will be worse the contacting.

3.3 Handling Precaution and Storage Notices

When using semiconductors, the incidence of thermal and/or mechanical stress to the devices due to improper handling may result in significant deterioration of their electrical characteristics and/or reliability.

Transportation

Be careful to handle the device and packaging material. Ensure that the device is not subjected to mechanical vibration or shock during transport. Do not toss or drop to ensure the device is O.K before on board. Wet condition is dangerous. Moisture can also adversely affect the packaging. Place the devices in the conductive trays before using. Hold the package and avoid touching the leads when handling devices. Do pay attention to the gate terminal. Put package boxes upside down, leaning them or giving them uneven stress might cause the electrode terminals to be deformed or the resin case to be damaged. Throwing or dropping the packaging boxes might cause the devices to be damaged. Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.

Storage

- Force or load the external pressure to the devices is not allowable.
- The storage area which will make the devices to be exposed to moisture or direct sunlight is not acceptable.
- The humidity should be kept within the range from 40% to 75%, and the temperature should be kept within the range from 5°C to 35°C.
- In the presence of harmful gases or in dusty conditions is not acceptable for storage.
- Lead solder ability will be degraded cause by lead oxidation or corrosion. So to use storage areas where there is minimal temperature fluctuation is highly recommended.
- Use antistatic containers. Unused devices should be stored no longer than one month when repacking devices.

Environment

- Use a board container or bag that is protected against static charge in case when storing device-mounted circuit boards.
- Do not stack them directly on top of one another, and keep them separated from each other, and to prevent static charge/discharge which occurs due to friction.

- Be sure cart surfaces that come into contact with device packaging are made of materials that will conduct static electricity, and are grounded to the floor surface with a grounding chain.
- To wear finger cots or gloves protected against static electricity if the human body comes into direct contact with a device,
- When humidity in the working environment decreases, the human body and other insulators can easily become charged with electrostatic electricity due to friction. Maintain the recommended humidity of 40% to 60% in the work environment. Be aware of the risk of moisture absorption by the products after unpacking from moisture-proof packaging.
- All equipment and tools in the working area are grounded to earth is necessary.
- Take other appropriate measures, or place a conductive mat over the floor of the work area, or so that the floor surface is grounded to earth and is protected against electrostatic electricity.
- Cover the workbench surface with a conductive mat, grounded to earth, to disperse electrostatic electricity on the surface through resistive components. Workbench surfaces must not be constructed of low-resistance metallic material that allows rapid static discharge when a charged device touches it directly.
- Ensure that work chairs are protected with an antistatic textile cover and are grounded to the floor surface with a grounding chain.
- Install antistatic mats on storage shelf surfaces.
- For transport and temporary storage of devices, use containers that are made of antistatic materials of materials that dissipate static electricity.
- Operators must wear antistatic clothing and conductive shoes (or a leg or heel strap).
- Operators must wear a wrist strap grounded to earth through a resistor of about 1MΩ.
- If the tweezers you use are likely to touch the device terminals, use an antistatic type and avoid metallic tweezers. If a charged device touches such a low-resistance tool, a rapid discharge can occur. When using vacuum tweezers, attach a conductive chucking pad at the tip and connect it to a dedicated ground used expressly for antistatic purposes.

Electrical Shock

- Do not touch the device unless you are sure that the power to the measuring instrument is off to avoid electrical measurement poses the danger of electrical shock for the device.

3.4 Marking Specification

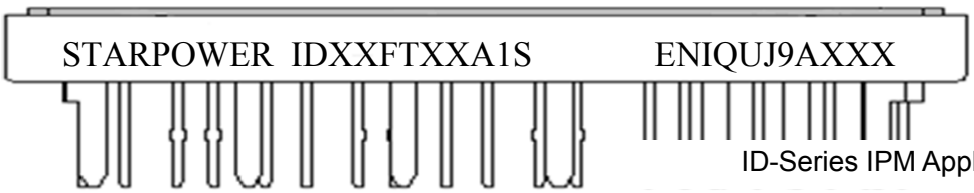


Figure 3-7. Marking Layout

1. IDXXFTXXA1S : ID series modeling ex:ID20FT06A1S sepc ID IPM 600V 20A
2. ENIQUJ9AXXX: Lot number ex:ENIQUJ9A003 ID 2009 08 3th Number

Chapter 4 Applications

4.1 System Connection Diagram

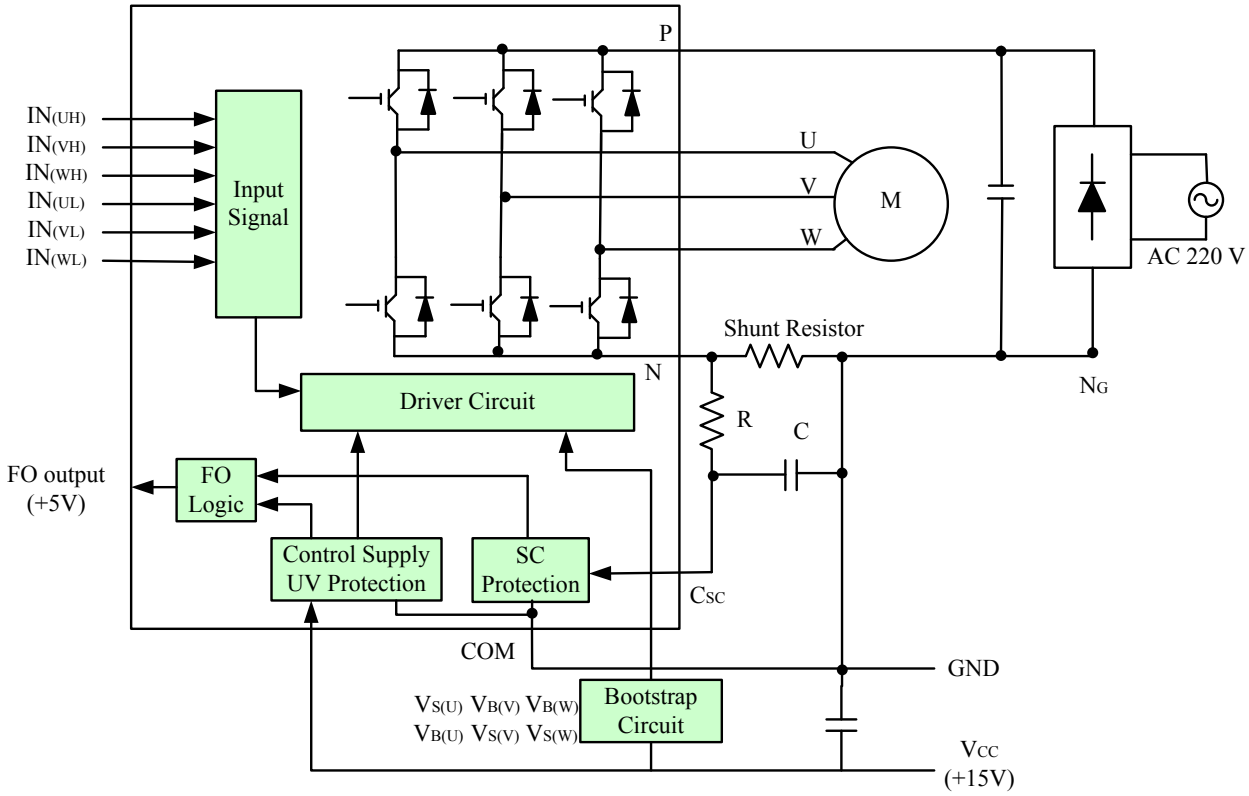


Figure 4-1. System Block Diagram of the IPM

4.2 Structure of Signal Input Terminals

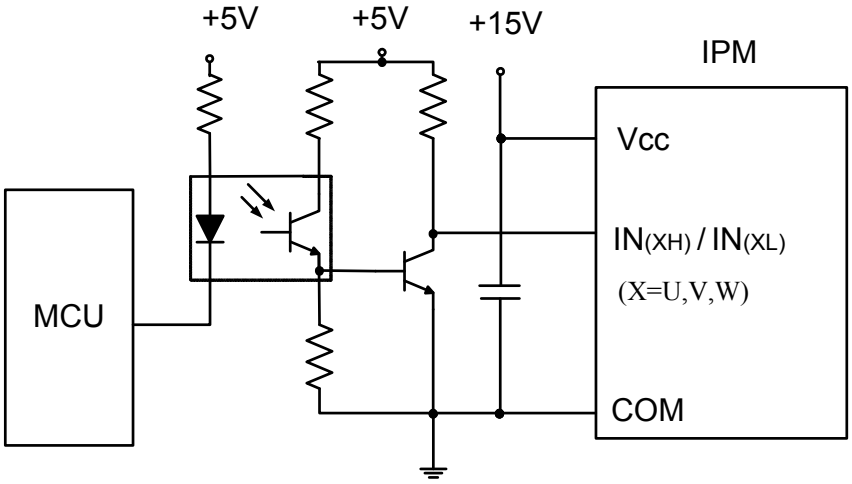


Figure 4-2. Interface Circuit Between ID-IPM and MCU

Note：RC coupling at each input may be changed depending on the PWM control scheme used in the application and on the wiring impedances of the application's PCB.

Signal Input and Fault Output

The structure of IPM signal input terminals is shown in Figure 4-2. The Fault output FO and input signals of the IPM should be a 5V-class interface. Therefore, if an opto-coupler is used, its supply voltage should be 5V. The maximum ratings for input and fault output voltages are shown in Table 4-1 and 4-2. As fault output is an open collector type and it's rating is 20.3V, 15V-class supply is possible. However, 5V-class supply is recommended for the fault output same as the input signals.

Table 4-1. Maximum Ratings of Input Signal and FO Pins Voltage

Item	Symbol	Condition	Ratings	Unit
Input signal voltage	$V_{IN(XH)}$ $V_{IN(XL)}$	Applied between $IN_{(XH)}$ – COM $IN_{(XL)}$ – COM	-0.3 ~ +5	V
Fault output voltage	V_{FO}	Applied between FO – COM	-0.3 ~ +5	V

Table 4-2. Value of Input Signal Current

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
$IN_{(UH / VH / WH)}$ input current	$I_{IN(HI)}$	$V_{IN(UH / VH / WH)}$ = 5V	-	100	200	μA
	$I_{IN(LO)}$	$V_{IN(UH / VH / WH)}$ = 0V	-1	-0.5	-	
$IN_{(UL / VL / WL)}$ input current	$I_{IN(HI)}$	$V_{IN(UL / VL / WL)}$ = 5V	-	100	200	
	$I_{IN(LO)}$	$V_{IN(UL / VL / WL)}$ = 0V	-1	-0.5	-	

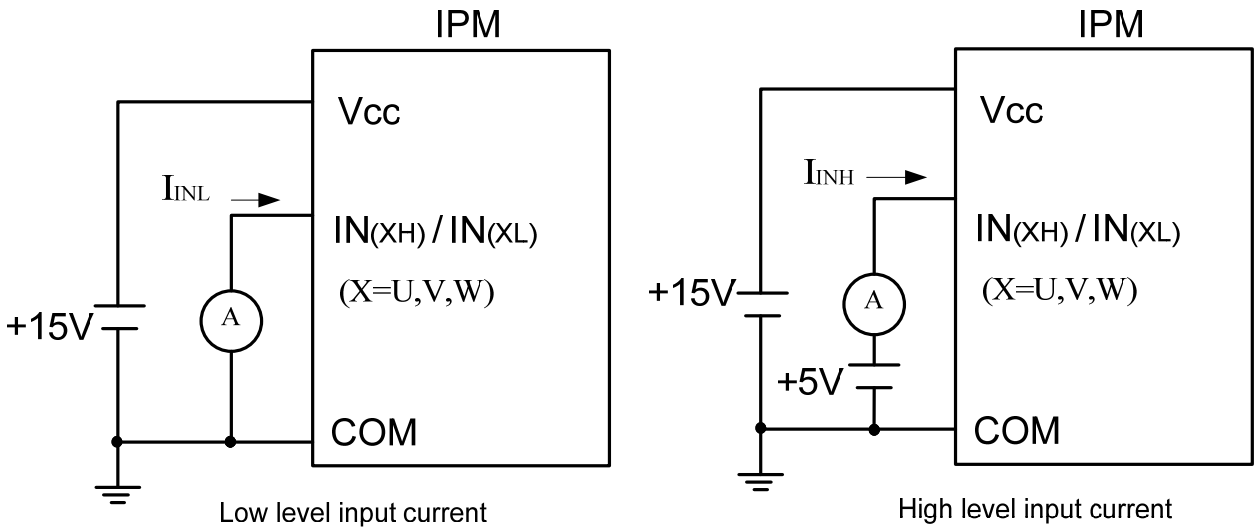


Figure 4-3. Diagram of Input Current Measurement Circuit

4.3 Bootstrap Circuit

Power for the high side gate drive is normally supplied using external bootstrap circuits. The bootstrap circuit typically consists of a low current 600V fast recovery diode with a small series resistor to limit the peak charging current and a floating supply reservoir capacitor. In order to avoid transient voltages and oscillations on the floating power supplies it is often desirable to add a low impedance film or ceramic type capacitor in parallel with each floating supply reservoir capacitor.

4.3.1 Operation of a Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between V_B and V_S, provides the supply to the driver IC within the IPM. This supply must be in the range of 10~20V to ensure that the driver IC can fully drive the high-side IGBT. The IPM includes an under-voltage detection function for the V_{BS} to ensure that the driver IC does not drive the high-side IGBT, if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode.

The bootstrap circuits is formed by an external ultra fast diode D_{BS}, capacitor C_{BS} and resistor R_{BS}. The bootstrap capacitor C_{BS} charges through the bootstrap diode D_{BS} and resistor R_{BS} from the V_{CC} supply when the high-side IGBT is off, and the V_S voltage is pulled down to ground. It discharges when the high-side IGBT is on. The current flow path of the bootstrap circuit is shown in Figure 4-4. It is necessary to apply an enough pulse width to fully charge the bootstrap capacitor C_{BS} and the timing chart of Initial bootstrap operation charging is shown in Figure 4-5.

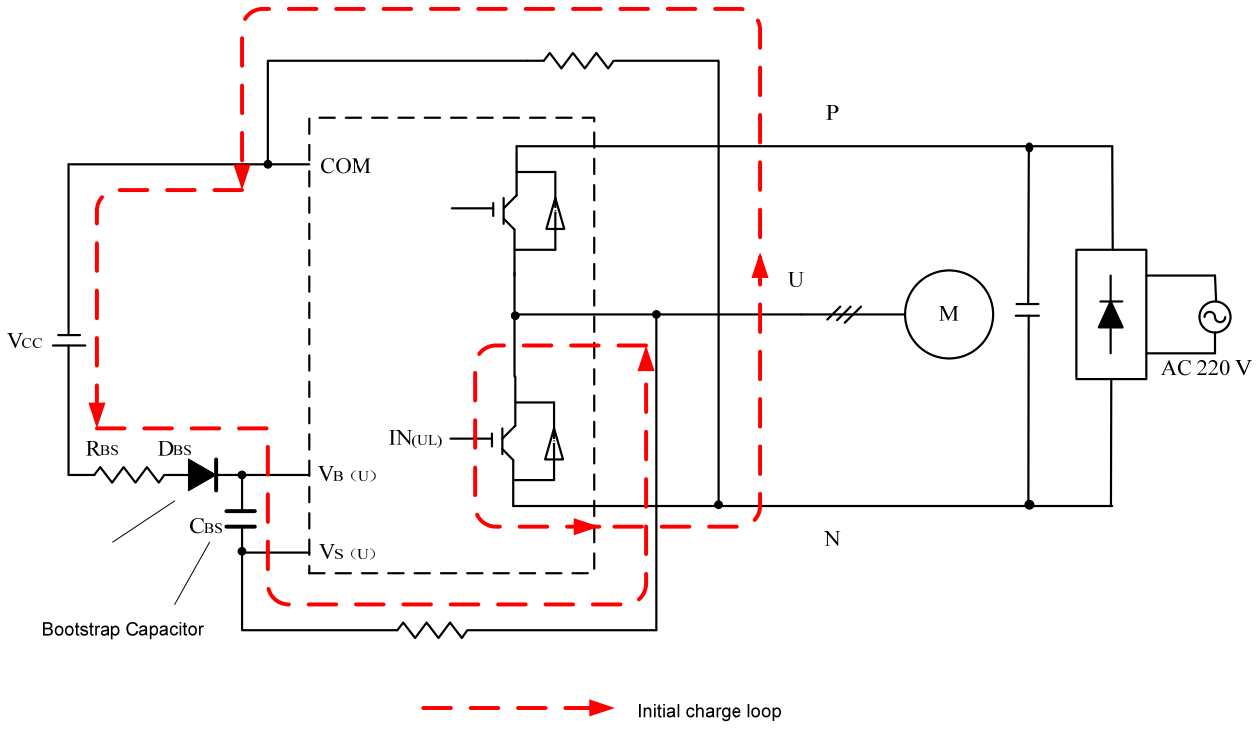


Figure 4-4. Bootstrap Circuit

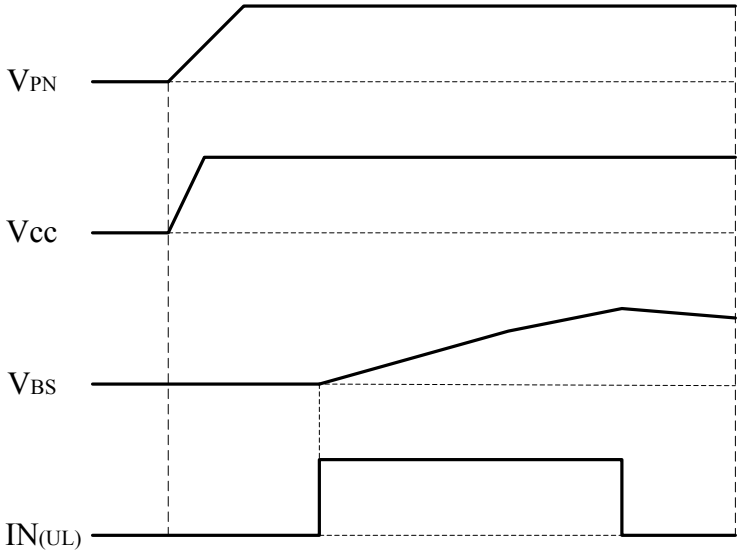


Figure 4-5. Timing Chart of Initial Bootstrap Operation Charging

The bootstrap capacitor charging and discharging timing chart is shown as Fig 4-7. We can see that the voltage V_{BS} is not a pure DC level and it has an inherently fluctuating voltage waveform because it is a floating supply due to bootstrap action.

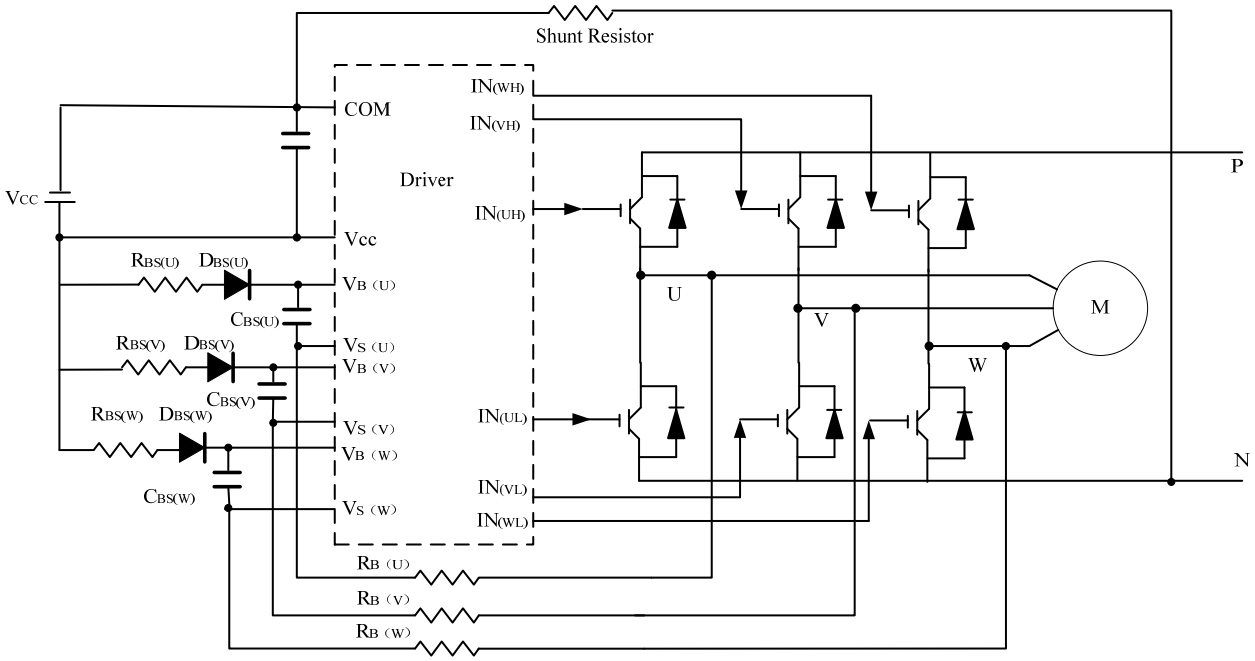


Figure 4-6. Inverter Circuit Diagram

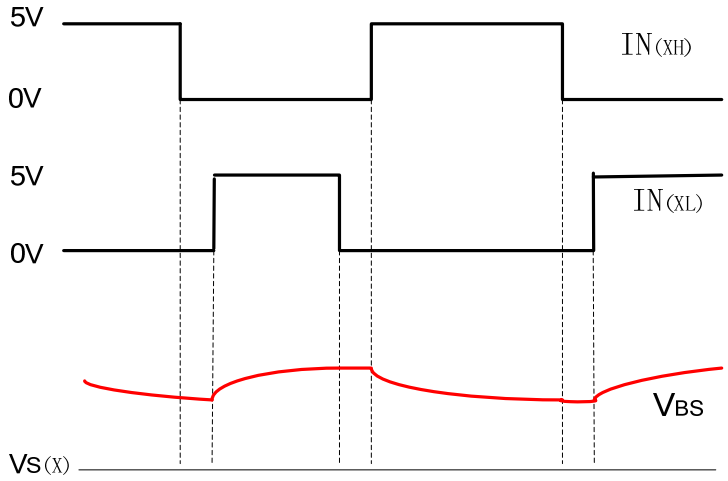


Figure 4-7. Charging and Discharging Action of the Bootstrap Capacitor Timing Chart

4.3.2 Initial Charging of a Bootstrap Capacitor

An adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time t_{charge} can be calculated from the following equation：

$$t_{charge} \geq C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{BS(min)} - V_F - V_{LS}}\right) \quad (4\text{-}1)$$

V_F = Forward voltage drop across the bootstrap diode
$V_{BS(min)}$ = The minimum value of the bootstrap capacitor
V_{LS} = Voltage drop across the low-side IGBT or load
δ = Duty ratio of PWM

4.3.3 Bootstrap Capacitor Selection

The voltage source of the bootstrap capacitor is the Vcc supply. Its capacitance is determined by the following constraints：

1、The gate charge required to enhance the IGBT.
2、I_{QBS} – Quiescent current for the driver IC.
3、Currents within the level shiftier of the driver IC.
4、Bootstrap capacitor leakage current.

Factor 4 is only relevant if the bootstrap capacitor is an electrolytic capacitor. It can be ignored if other types of capacitors are used. Hence, it is always better to use a non-electro ID-Series IPM Application Note tion describes the minimum charge, which needs to be supplied by the bootstrap capacitor：

$$Q_{BS} \geq Q_g + \frac{I_{GE(leakage)} + I_{CBS(leak)}}{f} + Q_{LS} \quad (4\text{-}2)$$

Q_g = Gate charge of the high-side of the IGBT
f = Switching frequency
$I_{CBS(leak)}$ = Bootstrap capacitor leakage current
$I_{GE(leakage)}$ = Gate to emitter leakage current for the driver IC
Q_{LS} = Level shift charge required per cycle = 5nC(built in driver IC)

The bootstrap capacitor must be able to supply this charge Q_{BS}, and retain its full voltage. Otherwise, there will be a significant amount of ripple on the V_{BS} voltage, which could fall below the V_{BSUV} (under-voltage detection level). Hence, it is recommended that the charge in the C_{BS} capacitor be at least twice the above value. Due to the nature of bootstrap circuit operation, a low value capacitor can lead to overcharging, which could in turn damage the driver IC. The minimum bootstrap capacitor value can be obtained from the following equation (4.3). Recommend to put the experienced value from 10uF~22uF.

$$C_{BS} \geq \frac{\left[Q_g + \frac{I_{GE(leakage)} + I_{CBS(leak)}}{f} + Q_{LS} \right]}{\Delta V} \tag{4-3}$$

Where ΔV = the allowable discharge voltage of the C_{BS}.

Note that the following equation (4.4) should be used for a specific system application, with an extended period of application of the standstill mode of the PWM output, during the changing of the rotor direction.

$$C_{BS} \geq I_{BS} \times \Delta T / \Delta V \tag{4-4}$$

Where ΔT is the maximum ON pulse width of IGBT1 and I_{BS} is the drive current of the driver IC (depends on temperature and frequency characteristics), and ΔV is the allowable discharge voltage.

The bootstrap capacitor should always be placed as close to the pins of the IPM as possible. A separate ceramic capacitor close to the IPM would be essential if an electrolytic capacitor were used for the bootstrap capacitor. Using a ceramic or tantalum type for the bootstrap capacitor, it should be adequate for local decoupling.

4.3.4 Series Resistor Selection

A resistor R_{BS} must be added in series with the bootstrap (ID-Series IPM Application Note the series resistor relative to the value of the bootstrap capacitor should be chosen such that the RC time constant is equal to or greater than 10us. Note that if the rising dV_{BS}/dt is slowed down significantly, it could temporarily result in a few missing pulses during the start-up phase due to insufficient V_{BS} voltage.

Resistor R_{BS} should be basically selected such that the time constant R_{BS} x C_{BS} will enable the discharged voltage ΔV being charged again into C_{BS} within the maximum ON pulse width of IGBT2, as show figure 4.7. However, if only IGBT1 has an ON-OFF-ON control mode, the time constant should be set so that the consumed charge during the ON period can be charged during the OFF period.

4.3.5 Bootstrap Diode Selection

The bootstrap diode D_{BS} is used for blocking the inverter DC-link voltage when the high-side device is switched “ON. So the bootstrap diode with withstand-voltage more than 600V is recommended. It is also important that the diode should be an ultra-fast recovery device to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{CC} supply. Similarly, the high temperature reverse leakage current would be important if the capacitor has to store a charge for long periods of time.

4.4 Application Circuit and Recommended Parts

4.4.1 Direct Input (without photo-Coupler) Interface Example

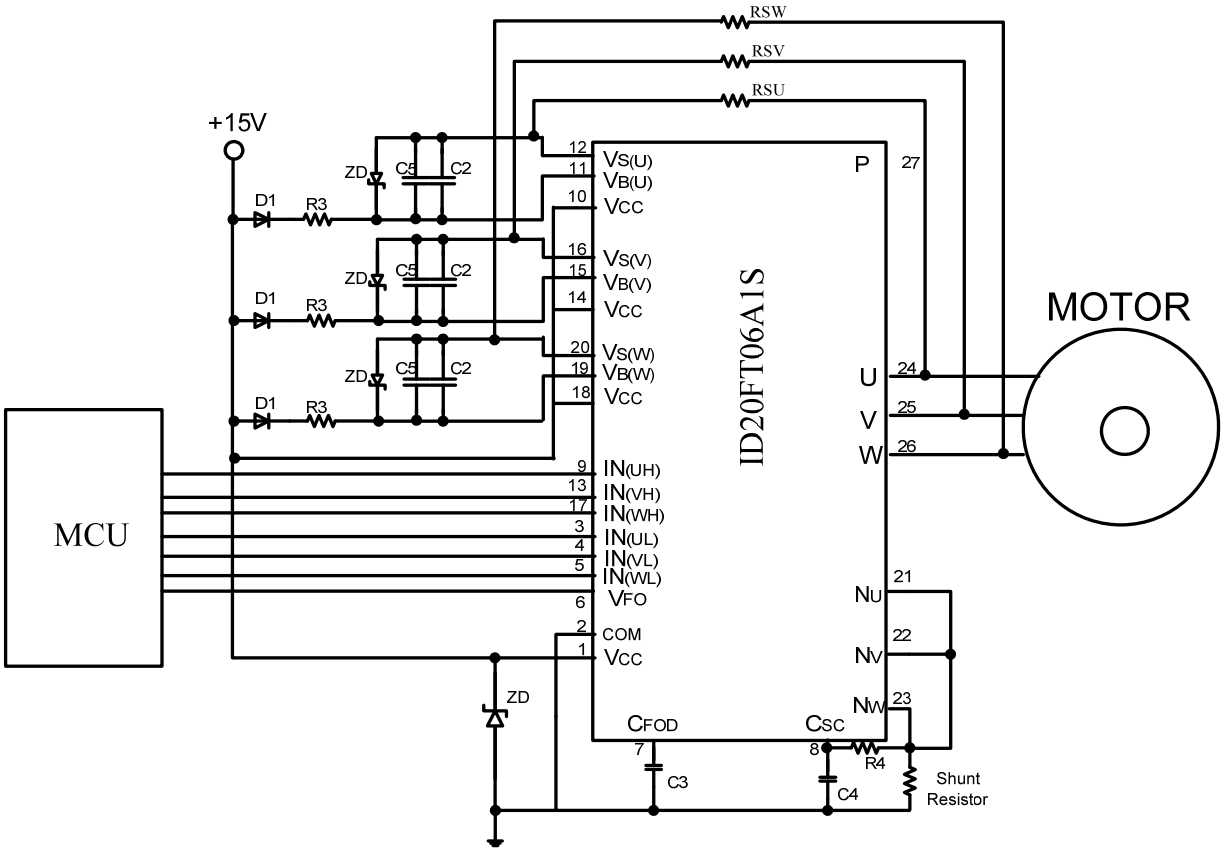


Figure 4-8. Typical Application Circuit Interface Example with Direct Input (Without Photo-Coupler)

Component selection:

1. R3 : 20Ω (It could be adjusted depending on the PWM frequency.)
2. R4 : 100Ω (Recommended the time constant R4xC4 is 2μS.)
3. C2 : 10 ~ 100μF (Electrolytic, low impendence)
4. C3 : 22~33nF (Ceramic)
5. C4 : 22~33nF (Ceramic)
6. C5 : 0.22 ~ 2μF (Ceramic)
7. D1 : 600V/1A (Ultra-Fast recovery diode)

4.4.2 Interface Example When a Photo-Coupler is Used

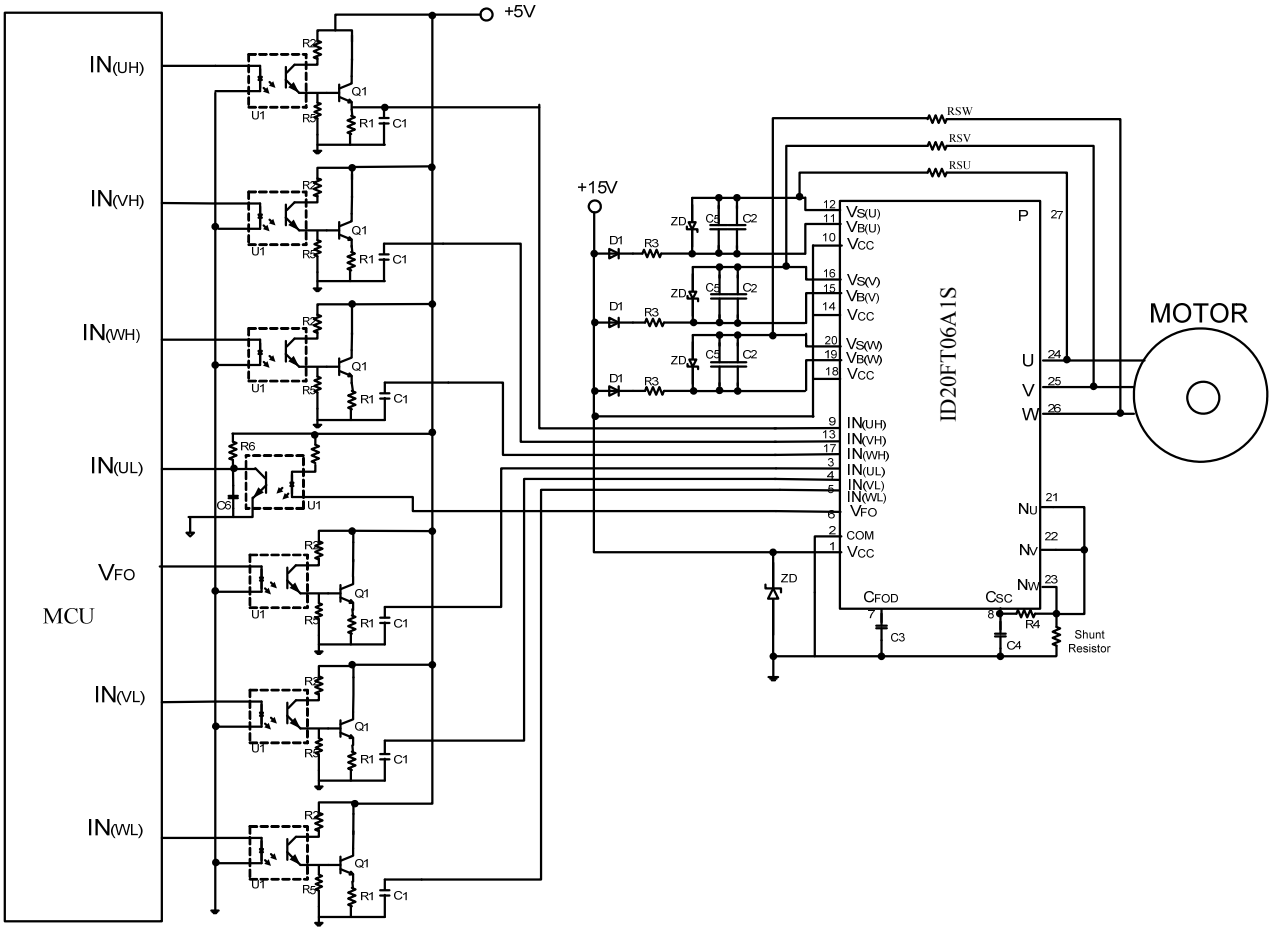


Figure 4-9. Typical Application Circuit Interface Example with Photo-Coupler

Component selection:

1.R1 : 4.7KΩ
2.R2 : 150Ω
3.R3 : 20Ω (It could be adjusted depending on the PWM frequency.)
4.R4 : 100Ω (Recommended the time constant R4xC4 is 2μS.)
5.R5 : 1KΩ
6.R6 : 1KΩ
7.R7 : 1KΩ
8.C1 : 0.1μF
9.C2 : 10 ~ 100μF (Electrolytic, low impendence)
10. C3 : 22~33nF (Ceramic)
11. C4 : 22~33nF (Ceramic)
12. C5 : 0.22 ~ 2μF (Ceramic)
13. C6 : 0.1μF
14. D1 : 600V/1A (Ultra-Fast recovery diode)
15. Q1 : NPN transistor 2N3904
16. U1 : Photo coupler TLP521

4.5 Input / Output Timing Diagram

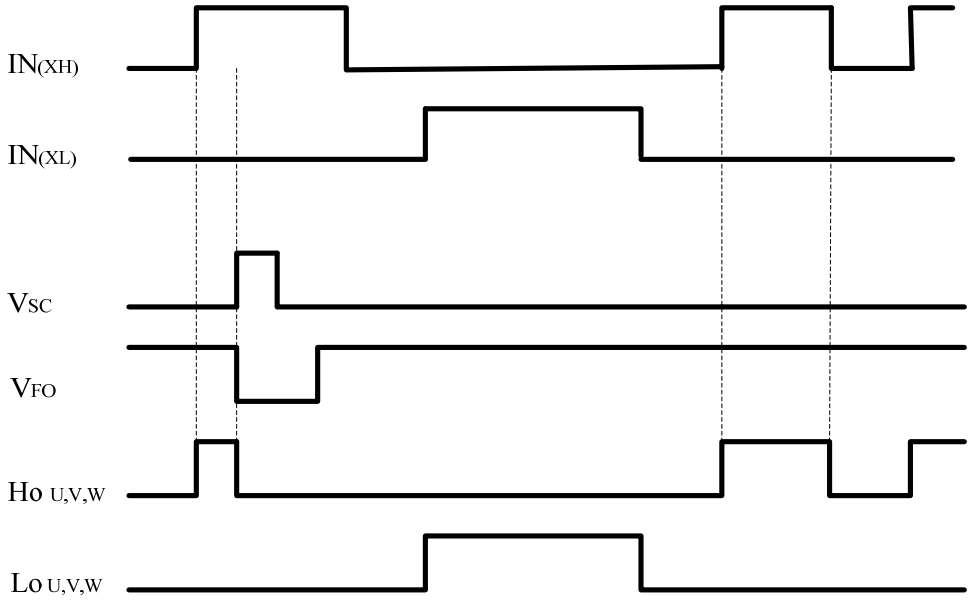
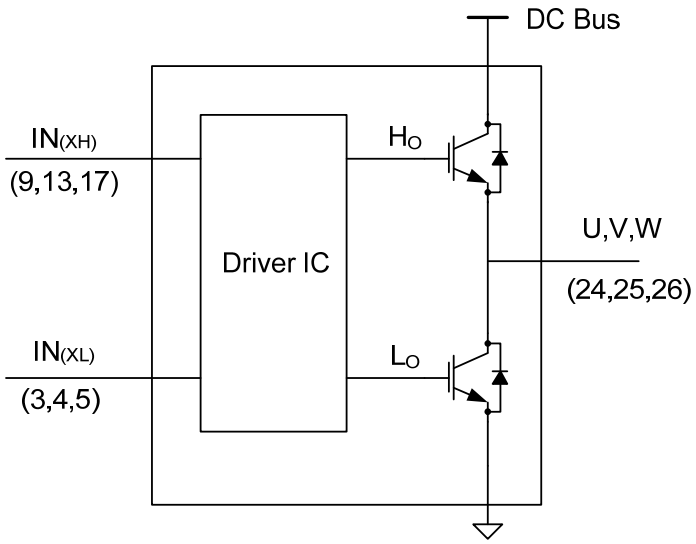


Figure 4-10. Input / Output Timing Diagram

Note：The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.



VSC	IN(XH)	IN(XL)	U,V,W
0	1	0	DC Bus
0	0	1	Vce(sat)
0	0	0	0

(X=U,V,W)

Figure 4-11. Input/Output Signal Circuit

4.6 Function and Protection Timing Charts

4.6.1 Timing Charts of Short Circuit Protection

(For the external shunt resistor and RC time constant circuit connected)

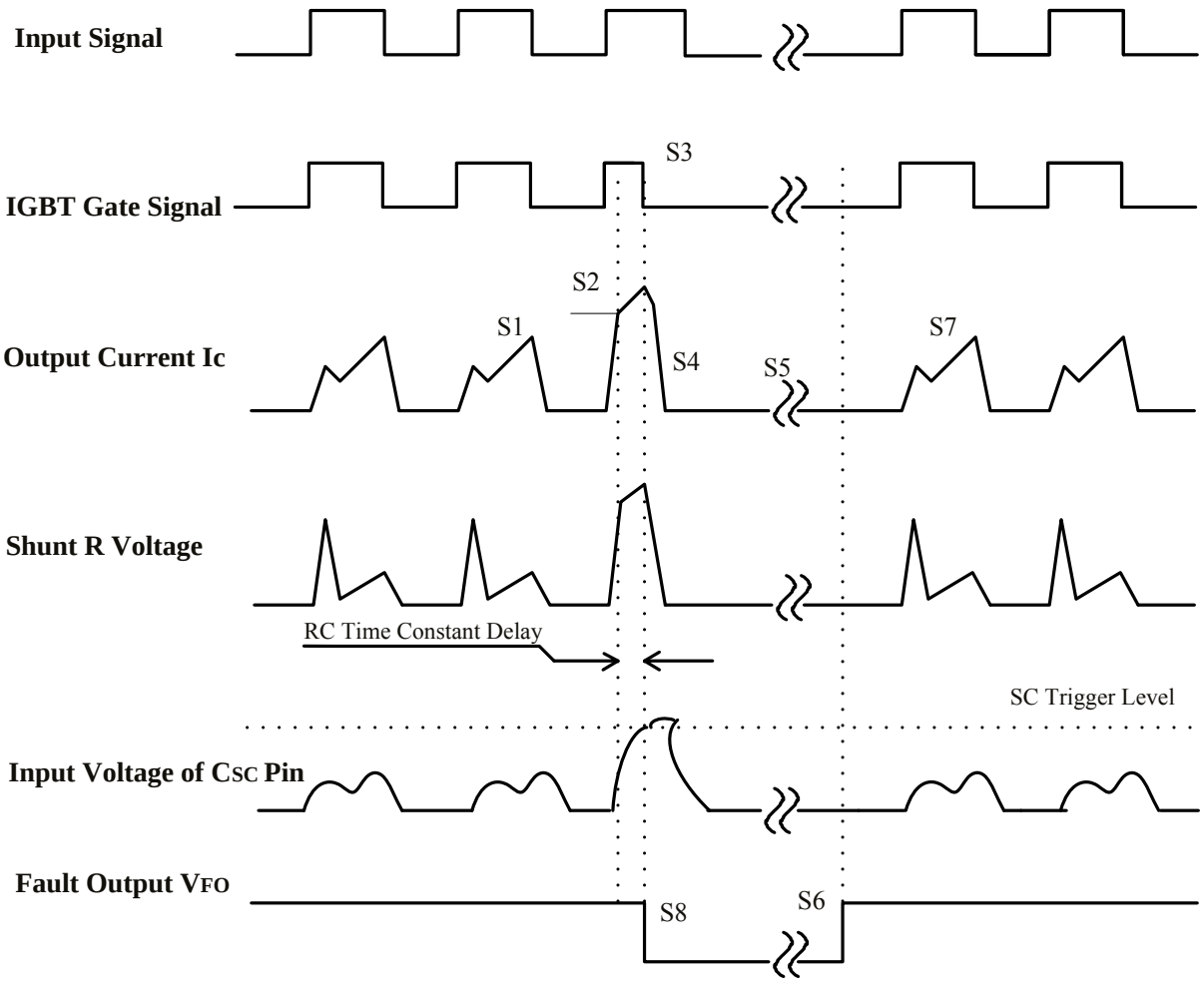


Figure 4-12. Timing Chart of SC Operation

S1. Normal operation : IGBT ON and carrying current.
S2. Short circuit current detection (SC trigger).

S3. Hard IGBT gate interrupt.
S4. IGBT turns OFF.
S5. IGBT OFF signal.
S6. IGBT ON signal - but IGBT cannot be turned on during the fault Output activation
S7. IGBT OFF state.
S8. Fault Output reset and normal operation start

4.6.2 Timing Charts of Under-voltage Protection

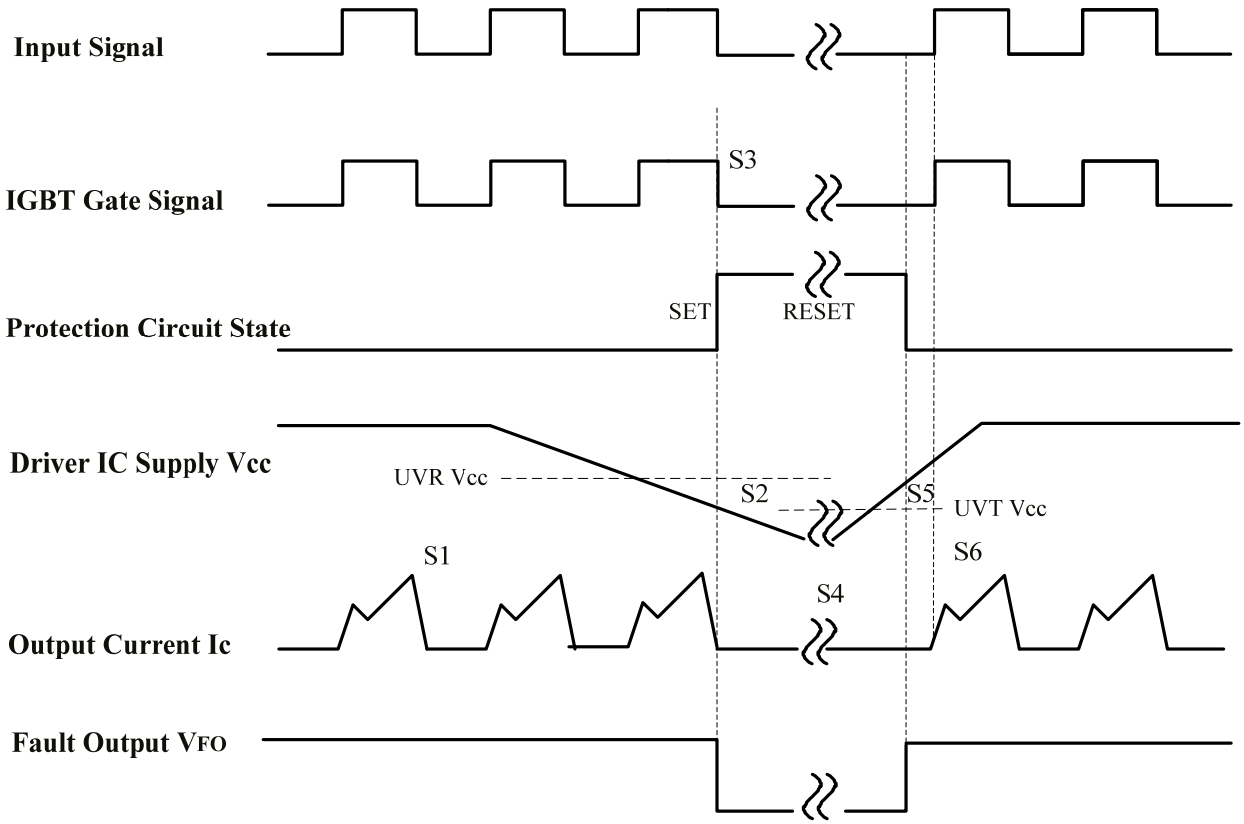


Figure 4-13. Timing Chart of Under-Voltage Operation

S1. Normal operation : IGBT ON and carrying current
S2. Under-voltage trip
S3. IGBT turns OFF inspire of control input condition
S4. FO timer operation starts : The pulse width of the FO signal is set by the external capacitor.
S5. Under-voltage reset
S6. Normal operation : IGBT ON and carrying current

4.6.3 Fault Output Loop

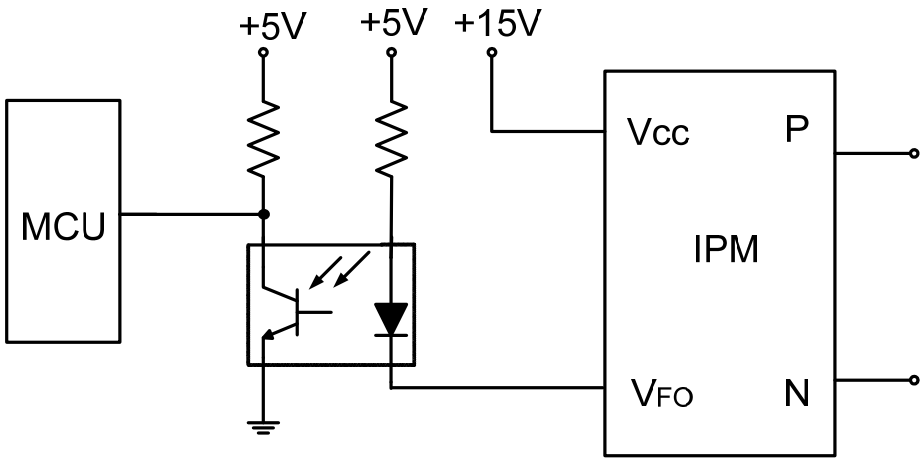


Figure 4-14. Diagram of FO pin Measurement Circuit

Table 4-4. Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Fault output voltage	VFO	Applied between VFO – COM	- 0.3 ~ VCC + 0.5	V
Fault output current	IFO		10	mA

Table 4-5. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	VFOH	VSC =0V，VFO =4.7kΩ to 5V	4.9	-	-	V
	VFOL	VSC =0.5V，VFO =4.7kΩ to 5V	-	-	0.2	V

4.6.4 Selecting the Current Sensing Shunt Resistor Value

The IPM short circuit protection accepts the voltage value across the external current sensing resistor into the internal driver IC as SC trip level (reference voltage) and operates by internally interrupting the output. The scheme for setting the value of external current sensing resistor is shown below：

- The current sensing resistor value is calculated using this expression：

$$R = V_{SC\ (ref)} / I_{SC}$$

Where $V_{SC\ (ref)}$ is the SC trip level (reference voltage) of the driver IC and I_{SC} is the current value to be interrupted

- The SC trip level (reference voltage) of the driver IC is designed based on the following specifications. Therefore, the fluctuation range (shown in Table 4-6.) should be taken into consideration.

- Figure 4-14. shows the relationship between sensing resistor values and interrupted current values, based on various conditions including fluctuation range described in Table 4-6.

- In the actual design, the filter circuit would be necessary and the sensing resistor value should be evaluated.

Table 4-6. Specification for $V_{SC\ (ref)}$

Condition	Min.	Typ.	Max.	Unit
$V_{SC(ref)}$ specification at T_a=25℃ (Typ.)	0.45	0.50	0.55	V

Example：

Sample NO.：ID20FT06A1S (20A/600V)

The maximum recommended short-circuit trip current is 1.7 times the nominal IC rating of the module：

Isc(max) = Ic(rating) × 1.7 = 20 × 1.7 = 34A

The minimum allowable shunt resistance is determined by requiring that the protection must operate at Ic = 34A, even if the modules short-circuit detection reference level (Vsc(ref)) is at its maximum. Referring to Table 4-6. for Vsc(ref) the minimum shunt resistance is：

Rshunt(min) = Vsc(ref)max / Isc =0.55 / 34 = 16.1 mΩ

If the tolerance of the shunt resistor is 5% then the possible range is：

Rmin = 16.1 mΩ, Rtyp = 17.0 mΩ, and Rmax = 17.8 mΩ

The typical short-circuit trip current is：

Isc(typ) = Vsc(ref)typ / Rtyp = 0.46 / 0.017 = 27.06A

The minimum short-circuit trip current is：

Isc(min) = Vsc(ref)min / Rmax = 0.37 / 0.0178 = 20.78A

Therefore, the range for short-circuit trip current is from 20.78A to 27.06A.

4.6.5 Filter Circuit Setting (RC Time Constant) for Short-Circuit Operation

Example of IPM Short-circuit Protection External Parts

The IPM have an integrated short-circuit protection function. The driver IC monitors the voltage across an external shunt resistor RSHUNT to detect excessive current in the DC link and provide protection against short circuits.

Figure 4-15 illustrates the typical external components used for sensing current. The voltage across RSHUNT is filtered by an RC circuit (R, C) and connected to the CIN pin. If the voltage at the CIN pin exceeds Vsc(ref), which is specified on the devices data sheets, then a fault signal is asserted and the arm IGBTs are turned off. The following sections will provide a detailed description of the over current protection function and external component selection.

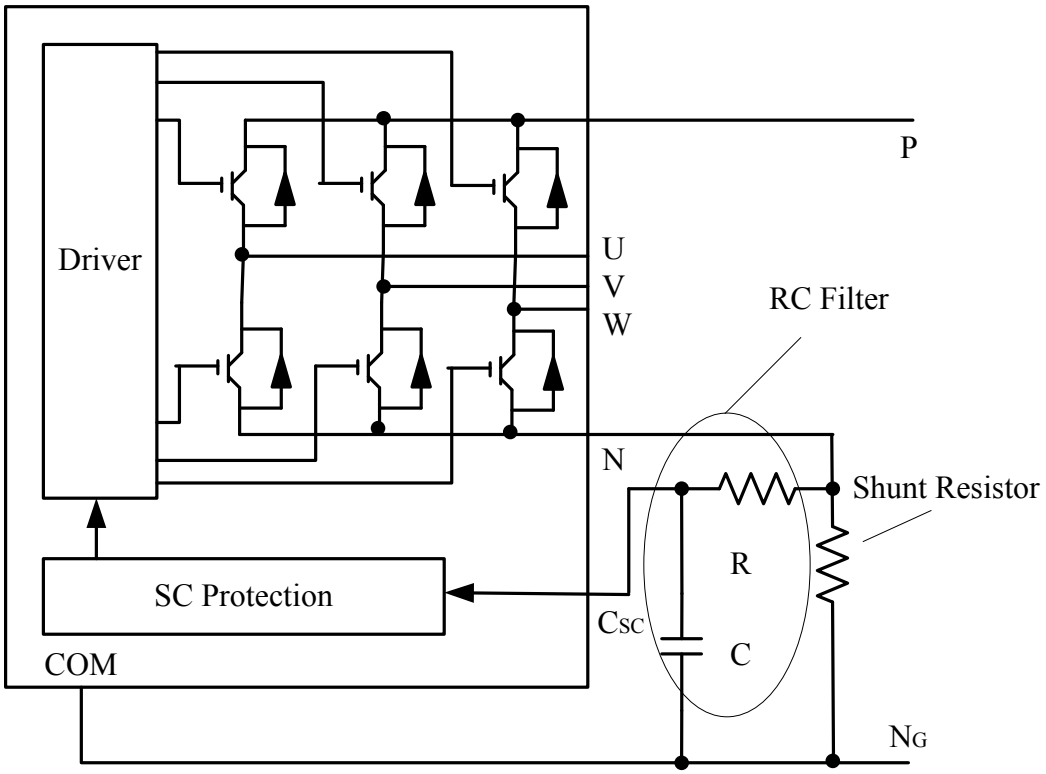


Figure 4-15. Example of External RC Filter Circuit

Figure 4-16 shows the example of external SC protection circuit. If the output current exceeds the SC trip level, all the gates of each IGBT are interrupted and the fault signal FO is outputted. The system operation should be stopped immediately when the fault output signal is pulled low.

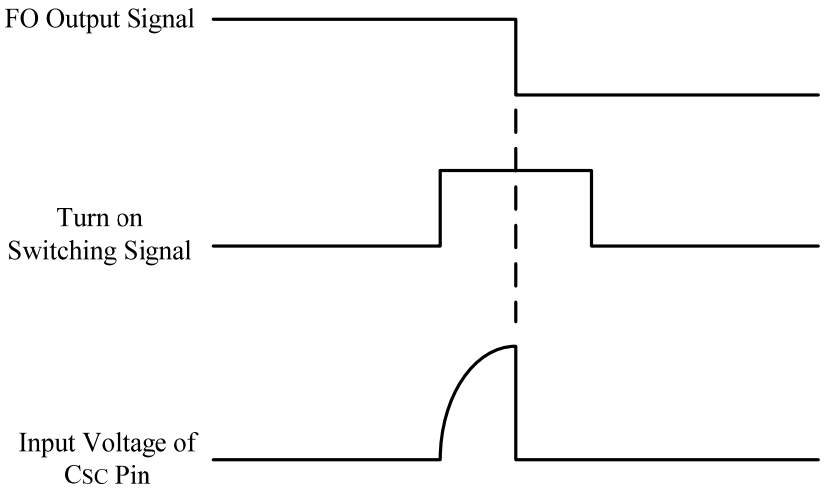


Figure 4-16. SC protection waveform

• Characteristics of RC Filter Circuit

When the RC filter circuit is connected, it can prevent the noise on the shunt resistor to make the SC protection

malfunction. The RC filter circuit immediately interrupts short-circuit currents due to its characteristics (shown in Figure4-17.) Figure 4-8 and Figure 4-9 show the recommended schemes for the different application of signal input. The RC time constant is determined depending on the applying time of noise interference and the withstand voltage capability of the IGBT.

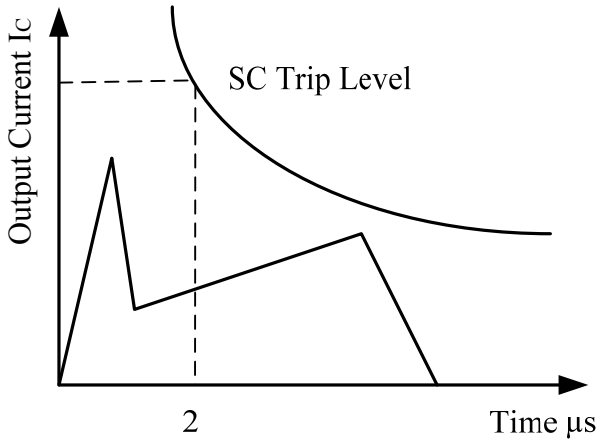


Figure 4-17. Characteristics of RC Filter Circuit

• Setting of RC Time Constant

An RC filter (R, C) should be inserted between the current sensing resistor and the IPM CIN pin as shown in Figure 4-15. The RC filter helps prevent erroneous fault detection due to di/dt noise on the shunt resistor and free-wheeling diode recovery current pulses. The RC filter also has the added advantage of producing a time dependent short-circuit trip level that responds quickly to severe low impedance short circuits and slowly to less dangerous overloads conditions. This characteristic is illustrated in Figure 4-17. The RC filter causes a delay in the short-circuit detection that must be coordinated with the short-circuit withstanding capability of the IGBT. For the IPM an RC time constant (τ = R x C) of 2 µ s or less is recommended to provide safe operation. A detailed description of the IGBT SOA and short-circuit withstanding capability is given in chapter 5.

Figure 4-11 is a timing diagram showing the operation of the short circuit protection. When current flows in the negative DC bus a voltage is developed across R_{SHUNT}. The voltage across R_{SHUNT} is filtered using an RC circuit consisting of R and C and connected to the CIN input on the IPM. If the collector current exceeds the Isc level for long enough to charge the shunt filter capacitor (C) to a voltage greater than Vsc(ref) (R_{SHUNT}). The filter (C, R) adds a time delay to prevent erroneous operation of the protection due to free-wheeling diode recovery currents and voltage surges caused by stray inductance in the sensing circuit. Selection of the shunt resistor and filter components will be covered in sections 4.6.4. When the protection is activated all IGBTs are turned off and the open collector fault output is pulled low. The IGBTs remain in the off state and the fault signal remains low for the duration of the fault timer (t_{FO}). The length of t_{FO} is set by the external timing capacitor C_{FO}. During this time the control input signals are ignored. Normal operation resumes at the first off-to-on transition following the end of the fault timer.

4.6.6 Recommend Wring of Snubber Circuit

• Snubber Circuit

In order to prevent ID-IPM from extra surge destruction, the wiring length between the smoothing capacitor and ID-IPM P-N terminals should be as short as possible. Also, a 0.1-0.22 μF/630 V snubber capacitor should be mounted in the DC-link close to ID-IPM.

There are three positions (A, B, C) to mount a snubber capacitor as shown in the fig.4-18.

If the snubber capacitor is installed in wrong location 'A' as shown in the Figure, the snubber capacitor cannot suppress the surge voltage effectively.

In order to suppress the surge voltage maximally, the wiring connect to the P port should be as short as possible when mounting a snubber capacitor outside the shunt resistor as shown in position B. If the sunbber capacitor is installed in the position B, that will suppress surge voltage effectively. However, the charging and discharging current generated by the wiring inductance and the snubber capacity will flow though the shunt resistor, which might cause erroneous protection if this current is large enough.

In a word, the "C" position surge suppression effect is greater than the location 'A' or 'B'. The 'B' position is a reasonable compromise with better suppression than in location 'A' without impacting the current sensing signal accuracy. For this reason, the location 'B' is generally used.

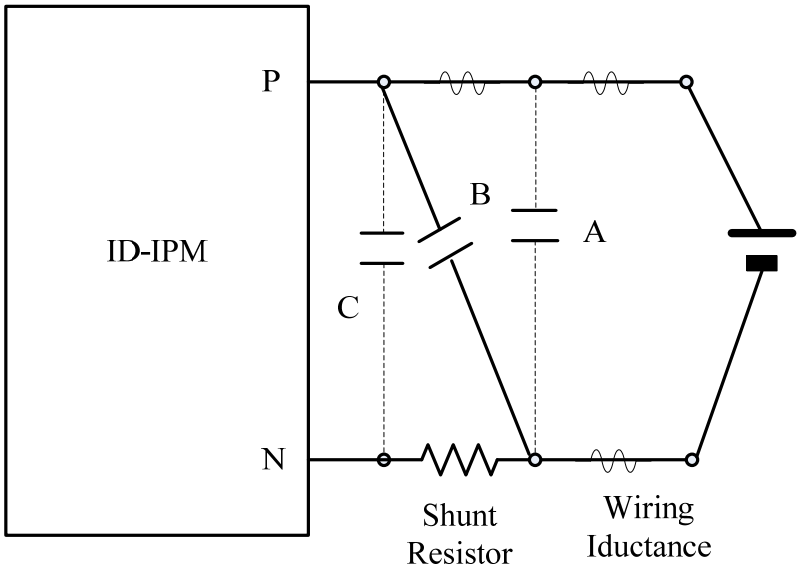


Figure 4-18. Recommended snubber circuit location

• Recommanded Wiring of Shunt Resistor

External shunt resistor is employed to detect short-circuit accident. A longer wiring between the shunt resistor and ID IPM might cause so much large surge that might damage built-in IC. To decrease the pattern inductance, the wiring between the shunt and ID IPM should be as short as possible, and using low inductance type resistor instead of long-lead type resistor.

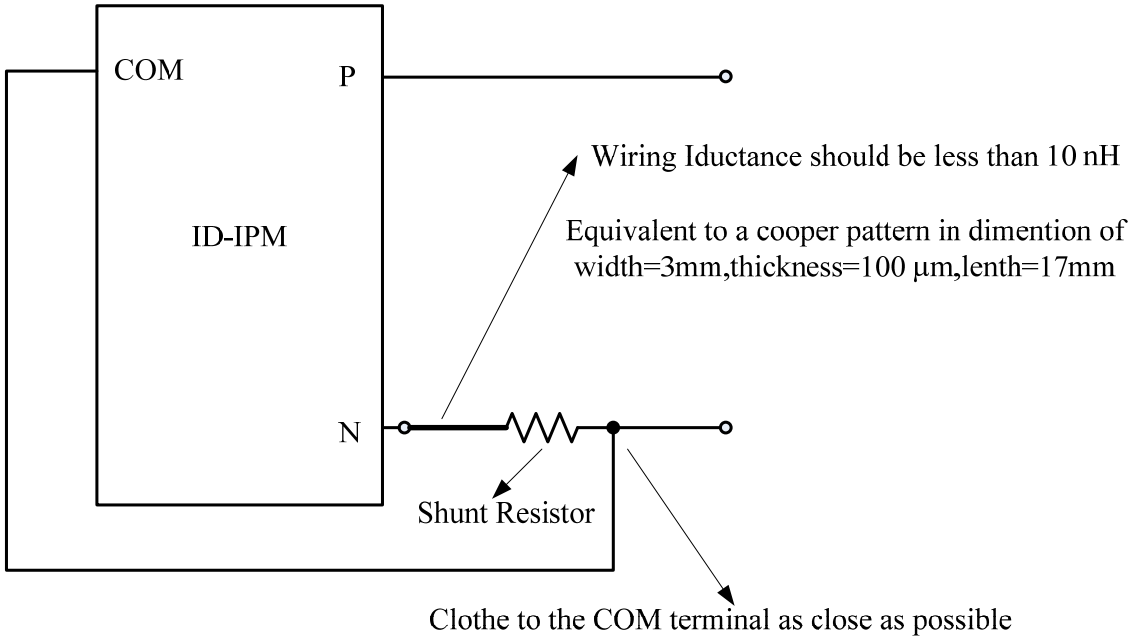


Figure 4-19. Recommend Wiring of Shunt Resistor

4.6.7 Parallel Connection

Figure 4-20 shows the circuit of parallel connection of two ID IPMs.

Rout H-loop and L-loop indicate the gate charging path of low-side IGBT in the ID IPM No.2. If the rout is too long, gate voltage might drop due to large voltage drop on the wiring, which will result a bad effect to the second IPM operation (Charging of bootstrap capacitor for high-side is similar, too.).

In addition, noise might easily impose to the wiring impedance. If there are many ID IPM parallel connection. COM pattern becomes long and the influence to other circuit (power supply, protection circuit etc.) by the fluctuation of COM potential is conceivable, therefore parallel connection is not recommended.

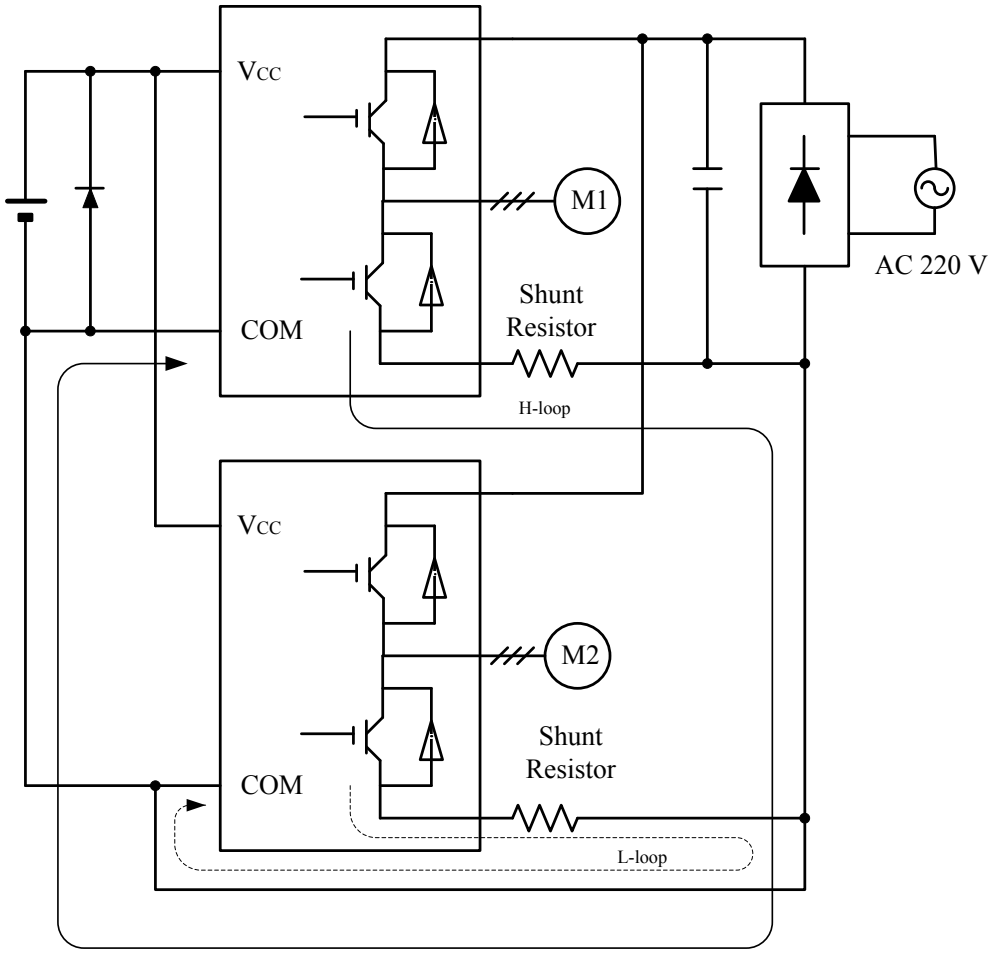


Figure 4-20. Parallel Connection

4.6.8 Trouble shooting of IPM

When using the IPM, some simple troubles can be monitor and shooting by table 4-7. By monitoring the V_{FO} pin signal, we can know when a protection occurs. Due to the build-in under-voltage and over-current protection function, When V_{FO} pin signal pulls down to ground, we should check which protection triggers.

• Under-voltage condition：

Check the Vcc whether is lower than 11.5V. By add the decoupling ceramic capacitor close to the Vcc pin could bypass some noise signal.

• Over-current condition：

Check whether a short circuit or over-current really happens. Some layout may cause the C_{SC} pin noise to mis-trigger. Approximately a 0.22~2μF by-pass capacitor should be used across each power supply connection terminals.

Table 4-7. Protection table

V_{CC}	V_{BS}	V_{SC}	V_{FO}
< U_{VCC}	X	X	0
15V	< U_{VBS}	0	0
15V	15V	0	H imp
15V	15V	> V_{trip}	0

Note：A shoot-through prevention logic prevents $L_{O1,2,3}$ and $H_{O1,2,3}$ for each channel from turning on simultaneously.
Note：U_{VCC} is not latched, when Vcc＞U_{VCC}, FO returns to high impedance.
Note：Over-current protection are latched protection and V_{FO} will turn high impedance after the fault condition recovery.

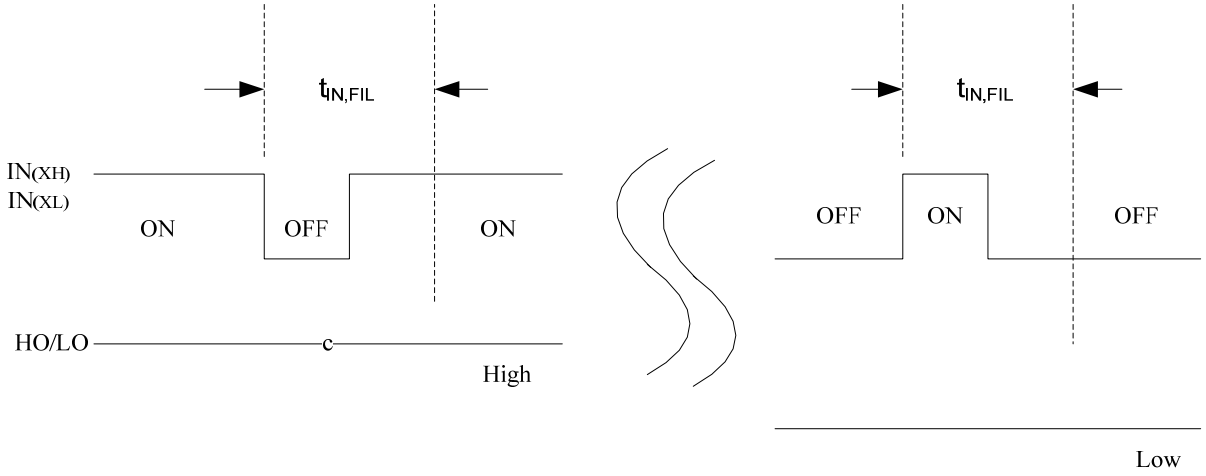


Figure 4-21. Input Filter Function

Note：For high side PWM, $IN_{(XH)}$ pulse width must be ≧ 1μsec.

Reference impedance for trouble shooting：(For ID20FT06A1S)

Table 4-7. ID IPM Impedance Measurement Range

ID IPM Impedance Measurement Range		
No.	Item	Reference impedance (ohm)
1	VCC,COM	>200M
2	$IN_{(UH)}$,$V_{S(U)}$	13.0M~15M
3	$IN_{(VH)}$,$V_{S(V)}$	13.0M~15M
4	$IN_{(WH)}$,$V_{S(W)}$	13.0M~15M
5	$IN_{(UH)}$,COM	25K~40K
6	$IN_{(VH)}$,COM	25K~40K
7	$IN_{(WH)}$,COM	25K~40K
8	$V_{B(U)}$, $V_{S(U)}$	1.5M~3.0M
9	$V_{B(V)}$, $V_{S(V)}$	1.5M~3.0M
10	$V_{B(W)}$, $V_{S(W)}$	1.5M~3.0M
11	C_{SC},COM	1.0 M ~1.5M
12	C_{FOD},COM	200K~500K
13	V_{FO},COM	35M~40M
14	P,N	Open
15	P,U	Open
16	P,V	Open
17	P,W	Open
18	U,N	Open
19	V,N	Open
20	W,N	Open

Chapter 5 Safe Operating Area

5.1 Safe operating area of the IPM

5.1.1 Definition of SOA

By built-in gate drive, under-voltage lockout and short-circuit protection guard them from many of the operating modes that would violate the Safe Operation Area (SOA) of the IGBTs in IPM. A conventional SOA definition that characterizes all possible combinations of voltage, current, and time that would cause power device failure is not required. In order to define the SOA for IPM, the power device capability and control circuit operation must both be considered. The resulting easy to apply switching and short-circuit SOA definitions for the IPM is summarized in this section.

The following describes the SOA (Safety Operating Area) of the IPM.

V_{CES} ： Maximum rating of IGBT collector-emitter voltage

V_{PN} ： Supply voltage applied on P-N terminals

V_{PN}(surge)： The add of V_{PN} and the surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{PN(PROT)}$： DC-link voltage that IPM can protect itself.

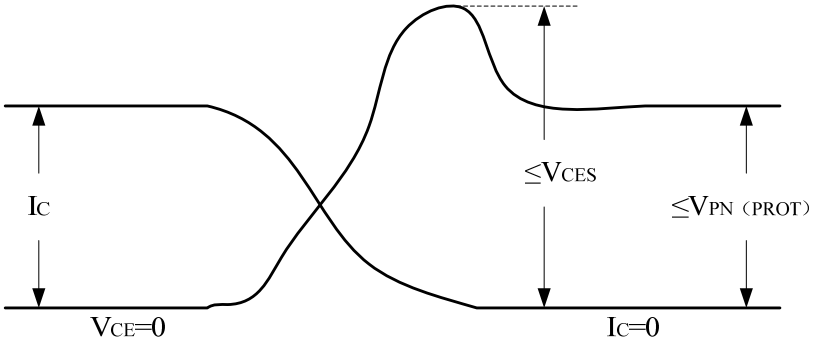


Figure 5-1. SOA for Switching

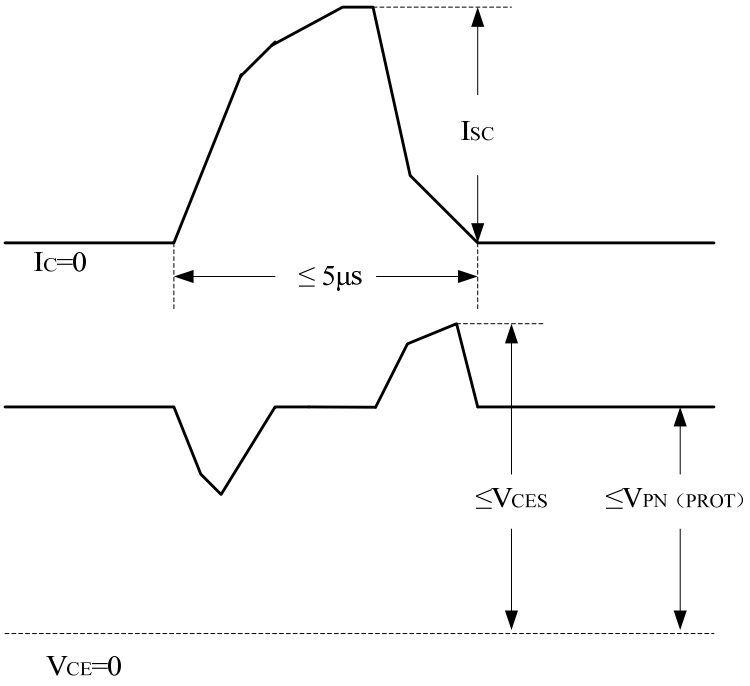


Figure 5-2. SOA for Short-circuit

5.1.2 Switching Operation

In fact, the V_{CES} represents the 600V voltage rating of the IGBTs incorporated into the IPM. But subtracting the surge voltage generated by the stray inductance of the PCB trace and the internal wire bonding of the IPM. Moreover, subtracting from V_{PN}(Surge) the surge voltage generated by the stray inductance between the IPM and the DC-link capacitor is V_{PN} (Surge), please refer to the data sheet for the rated surge voltage .

1. FBSOA – Turn on transition (Power dissipation limited)
2. RBSOA – Turn off transition (Latch-up spec)

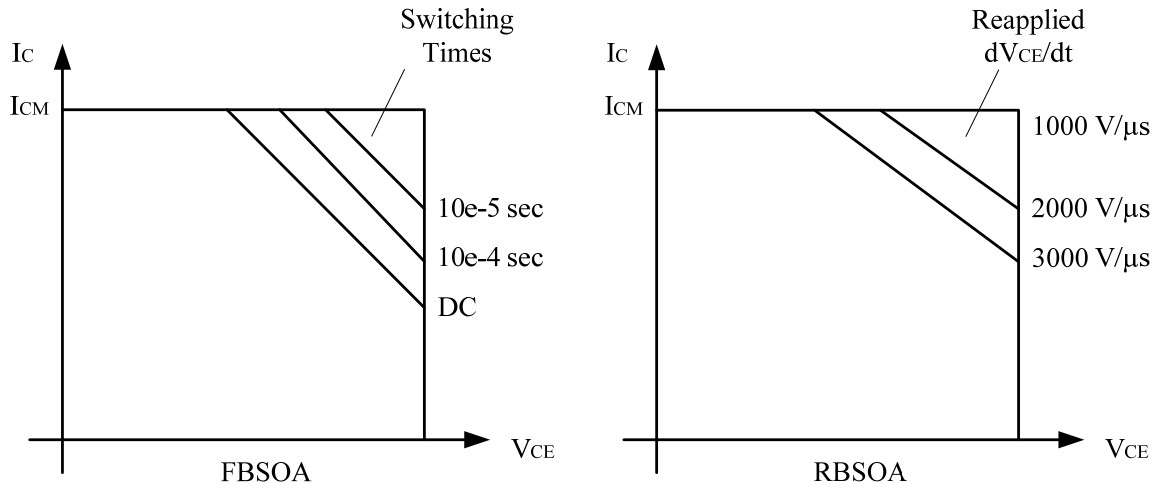


Figure 5-3. Safe Operating Area During Switching

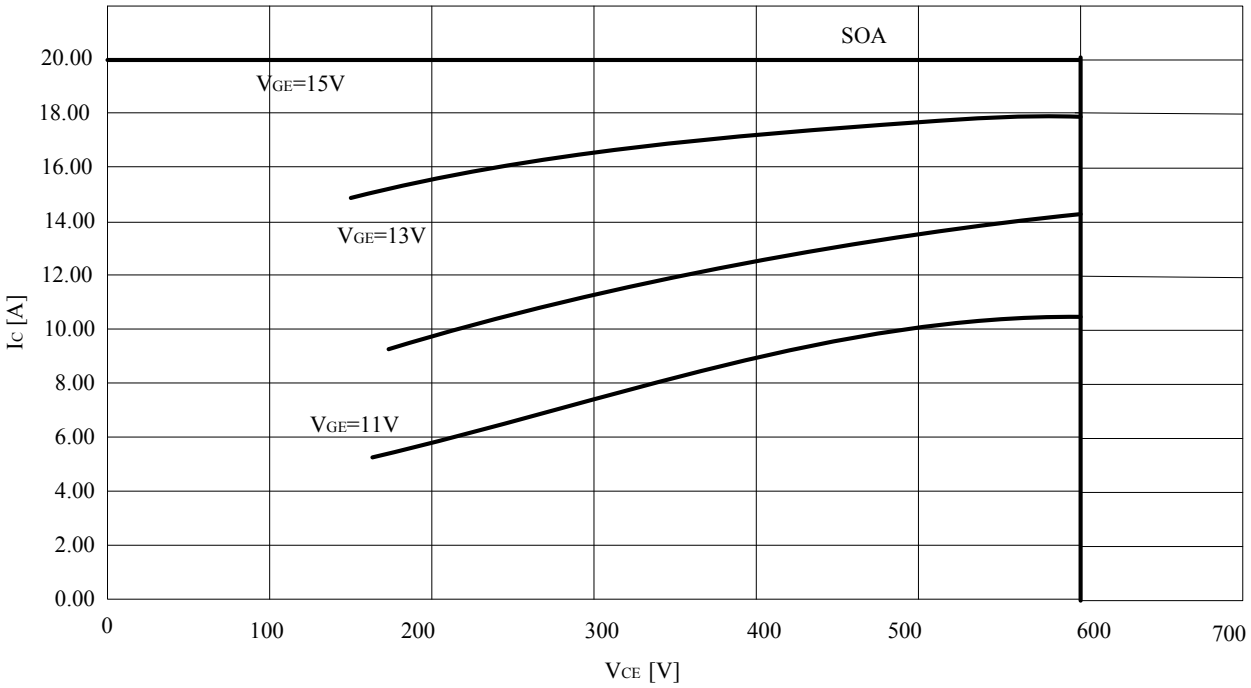


Figure 5-4. Safe Operating Area During Short-Circuit (SCSOA)

V_{CES} represents the 600V voltage rating of the IGBTs incorporated into the IPM. Subtracting the surge voltage (100V or less), generated by stray inductance inside the IPM, from V_{CES} is V_{PN}(Surge), that is, 500V. Moreover, subtracting from V_{PN} (Surge) the surge voltage (100V or less) generated by the stray inductance between the IPM and the DC-link capacitor is $V_{PN(PROT)}$, that is 400V.

Table 5-1. The Absolute Maximum Rating of P-N Voltage

Items	Symbol	Condition	Rating	Unit
Supply Voltage	V_{PN}	Applied to P-N	450	V
Supply Voltage (Surge)	$V_{PN\ (Surge)}$	Applied between P-N	500	
Collector - Emitter Voltage	V_{CES}		600	
Self protection Supply Voltage Limit (Short-circuit Protective Capability)	$V_{PN(PROT)}$	Applied to DC link, Tj = 125℃, Vcc = V_{BS} = 11.5V ~ 20.0V, Non-Repetitive, less than 5us	400	

Note：It is recommended that the average junction temperature should be limited to Tj≦150° C (@ TC≦100° C) in order to guarantee safe operation.

5.2 Noise Immunity Capability

Figure 5-5 shows noise immunity capability testing circuit, ID-IPM have been confirmed to be with ±2KV noise immunity capability, Noise immunity capability extremely depend on the testing system environment , component layout, control substrate patterns, and other factor, so an additional confirmation on prototype is necessary .

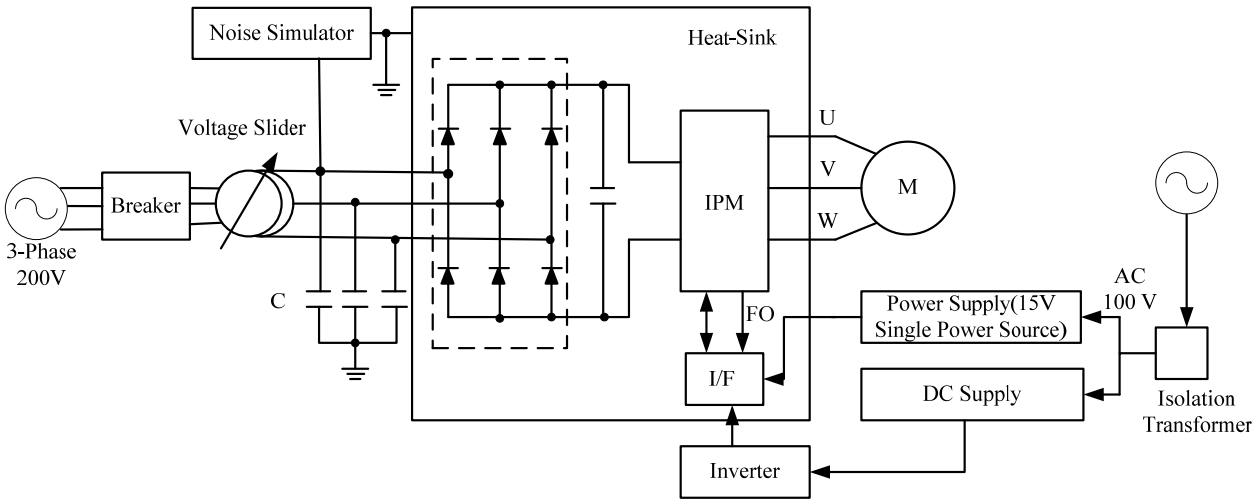


Figure 5-5. Noise test circuit

Note：

C：AC line common-mode filter 4700pF

PWM signals are inputted from microcomputer both directly and through opto-coupler

15V single power-source drive

Test is performed for both IM and DCBLM motors

Test conditions：

VCC=300V,VD=15V,Ta=25° C, no load.

50ns~1us wide pulses are applied at a random point each 60Hz cycle.

5.3 ESD withstand capability

ID-IPM has been confirmed to be with ± 250V or more withstand capability under the above evaluation circuit.

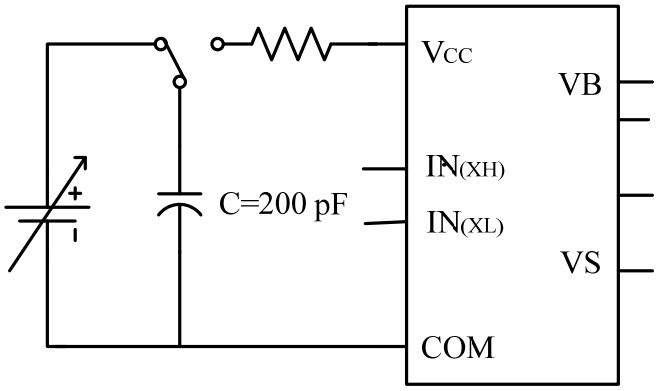


Figure 5-6. ESD Test Circuit (insides IC)

Qualification Level：Industrial level. MSL3, Lead-free.

ESD Classification：

Human Body Model(HBM)：Class2,per JESD22-A114-B

Machine Model(MM)：Class B, per EIA/JESD22-A115-A

Chapter 6 Reference Design

6.1 Demo board introduction

- **Demo board schematic**

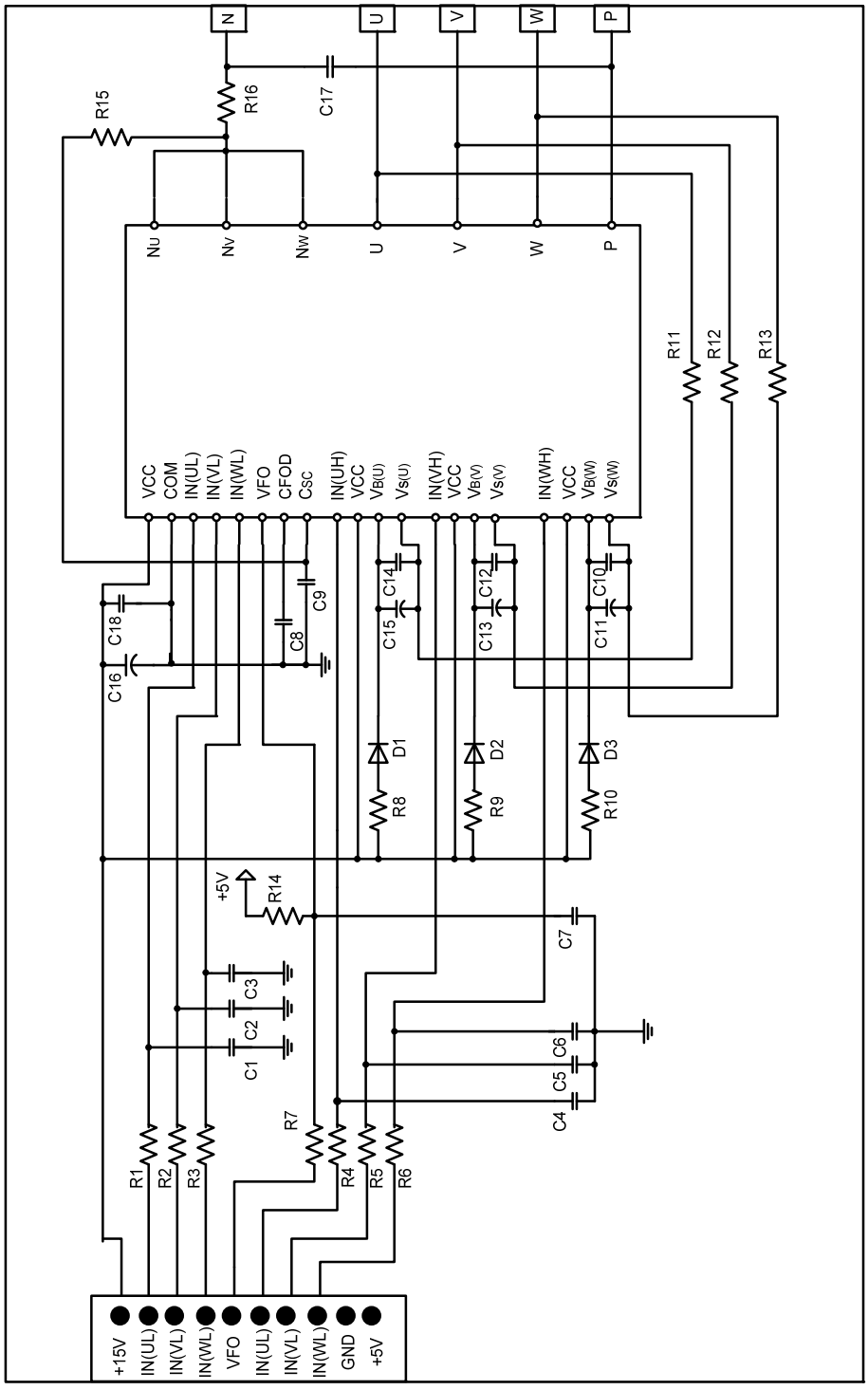


Figure 6-1. Demo Board Schematic

- **Demo board layout**

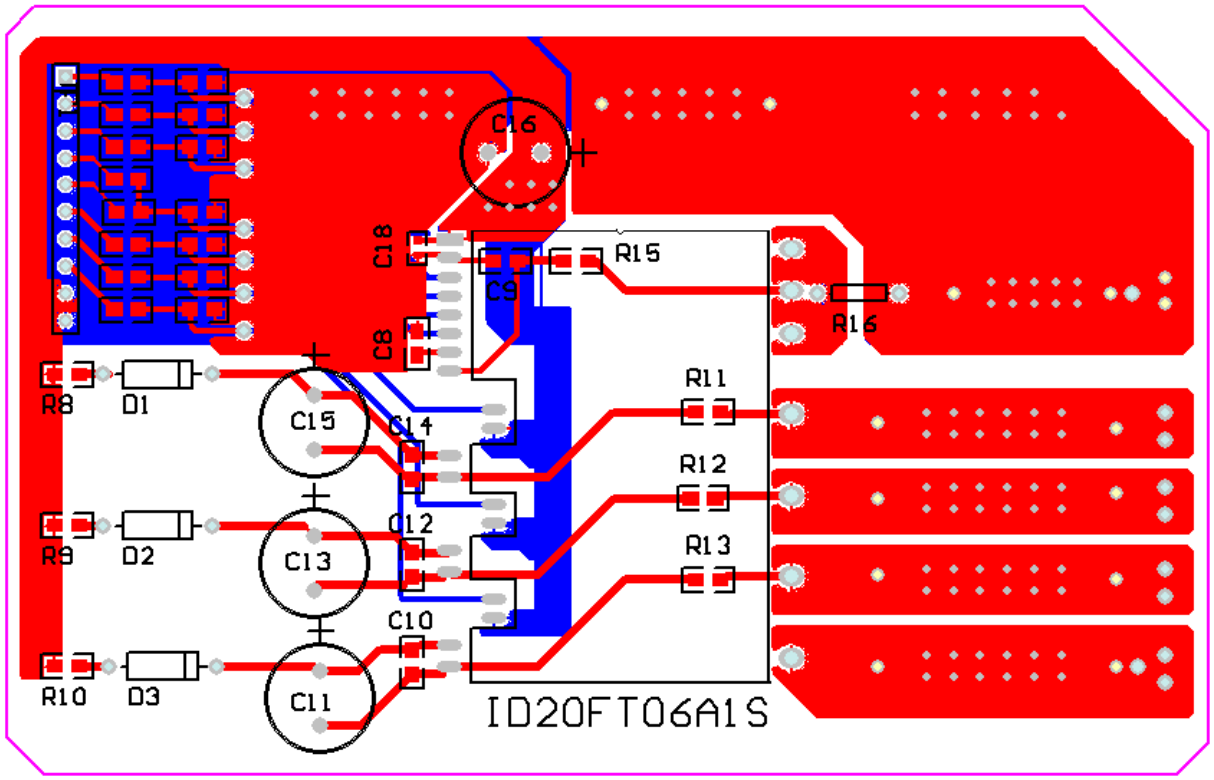


Figure 6-2.Demo Board Toplayer

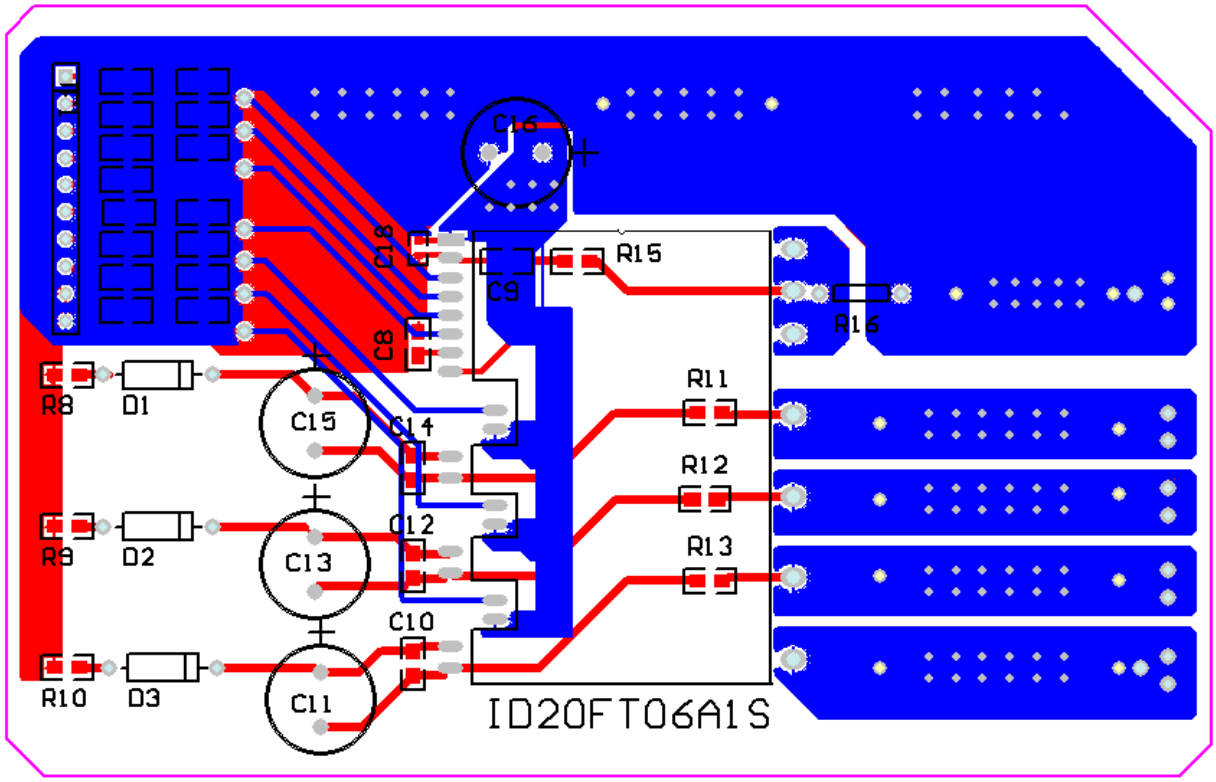


Figure 6-3.Demo Board Bottomlayer

- **Bill of Materials**

Table 6-1.Demo-Board B.O.M List

Used	Part Type	Rating	Characteristics	Definition
1	C1	1 nF	Ceramic Capacitor	Low-Side Pull-Down Capacitor
2	C2	1 nF	Ceramic Capacitor	Low-Side Pull-Down Capacitor
3	C3	1 nF	Ceramic Capacitor	Low-Side Pull-Down Capacitor
4	C4	1 nF	Ceramic Capacitor	High-Side Pull-Down Capacitor
5	C5	1 nF	Ceramic Capacitor	High-Side Pull-Down Capacitor
6	C6	1 nF	Ceramic Capacitor	High-Side Pull-Down Capacitor
7	C7	1 nF	Ceramic Capacitor	+5V Bias Voltage Bypass Capacitor
8	C8	33 nF	Ceramic Capacitor	Capacitor for Selection of Fault Out Duration
9	C9	1 nF	Ceramic Capacitor	Bypass Capacitor for Current Sensing
10	C10	100 nF	Ceramic Capacitor	Bypass Capacitor for Bootstrap Supply (Phase U)
12	C11	6.8 uF 35 V	Electrolytic Capacitor	Bootstrap Capacitor (Phase U)
13	C12	100 nF	Ceramic Capacitor	Bypass Capacitor for Bootstrap Supply (Phase V)
14	C13	6.8 uF 35 V	Electrolytic Capacitor	Bootstrap capacitor (Phase V)
15	C14	100 nF	Ceramic Capacitor	Bypass Capacitor for Bootstrap Supply (Phase W)
16	C15	6.8 uF 35 V	Electrolytic Capacitor	Bootstrap capacitor (Phase W)
17	C16	220 uF 35V	Electrolytic Capacitor	+15V Bias Voltage Source Capacitor
18	C17	100 nF 630V	Film Capacitor	Snubber Capacitor to Suppress the Spike-Voltage
19	C18	1uF 35V	Ceramic Capacitor	+15V Bias Voltage Bypass Capacitor
20	R1	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (UL)
21	R2	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (VL)
22	R3	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (WL)
23	R4	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (UH)
24	R5	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (VH)
25	R6	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (WH)
26	R7	100Ω 1/8 W	Carbon Film Resistor	Series Resistor for Signal Interface (Fault-out)
27	R8	20Ω 1/4 W	Carbon Film Resistor	Bootstrap Resistor (Phase U)
28	R9	20Ω 1/4 W	Carbon Film Resistor	Bootstrap Resistor (Phase V)
29	R10	20Ω 1/4 W	Carbon Film Resistor	Bootstrap Resistor (Phase W)
30	R11	5.6Ω 1/4 W	Carbon Film Resistor	Emitter Resistor for Switching
31	R12	5.6Ω 1/4 W	Carbon Film Resistor	Emitter Resistor for Switching
32	R13	5.6Ω 1/4 W	Carbon Film Resistor	Emitter Resistor for Switching
33	R14	4,7KΩ 1/8 W	Carbon Film Resistor	Pull-up Resistor (Fault output)
34	R15	1.8 KΩ 1/8 W	Carbon Film Resistor	Low-pass-Filter for Current Sensing


35	R16	20mΩ 5 W	Non-inductive Resistor	Shunt Resistor for Current Sensing
36	D1	1A 600V	Fast Recovery Diode	Bootstrap Diode (Phase U)
47	D2	1A 600V	Fast Recovery Diode	Bootstrap Diode (Phase V)
48	D3	1A 600V	Fast Recovery Diode	Bootstrap Diode (Phase W)

6.2 Layout Guide-line

- It is recommended that the wiring of the DC- link power path be as short as possible.
- To suppress surge voltage, a non-inductive snubber capacitor should be mounted as close to P and GND (shunt resistor's return pins) as possible.
- The wiring of N terminal and shunt resistors should be as short as possible and shunt resistors' pin connected DC-link GND also should be as short as possible.
- To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible.
- To minimize the pattern impedance, it is recommended that the bootstrap current path be as short as possible.
- FO output is open collector type. The signal line should be pulled up the positive side of the 5V power supply with approximately 4.7kΩ resistance.
- FO output pulse width should be decided by connecting an external capacitor between CFO and GND terminals.
- Each input signal line should be pulled up to the 5V power supply with approximately 680Ω~4.7kΩ resistance. Approximately a 0.22~2μF by-pass capacitor should be used across each power supply connection terminals.
- In order to provide good decoupling between Vcc-GND and V_B-V_S terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically 0.1μF, are strongly recommended in order to achieve strong noise immunity.
- High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.
- Each capacitor should be put as nearby the pins of the IPM as possible.

Chapter 7 Thermal Resistances Concepts Introduction

7.1 Overview

Semiconductor devices are very sensitive to junction temperature, i.e., as the junction temperature increases, the operating characteristics of a device are altered from normal, and the failure rate increases exponentially. This makes the thermal design of the package a very important factor in the device development stage, and also in an application field.

To gain insight into the device's thermal performance, it is normal to introduce thermal resistance. The thermal resistance is a measure of the temperature change across a package caused by power dissipation of the packaged semiconductor device. It is an indication of the heat transfer from the semiconductor device through the package materials out to the environment in terms of temperature per unit of power. Thermal resistance data can be used by the de-signer or customer to estimate the junction temperature of their die in operation.

Figure 7-1 shows a thermal network of heat flow from junction-to-ambient for the SDIP-IPM including a heat sink.

The thermal resistance of the ID-IPM is defined in the following equation.

The thermal resistance of a semiconductor device is generally as：

$$R_{\theta JX} = \frac{T_J - T_X}{P_H} \tag{7-1}$$

Where $R_{\theta JX}$ = Thermal resistance from device junction to the specific environment (alternative symbol is θ_{JX}) [℃/W]

T_J = device junction temperature in the steady state test condition [℃]

T_X = reference temperature for the specific environment [℃]

P_H = power dissipated in the device [W]

The selection of a reference point is arbitrary, but usually the hottest spot on the back of a device on which heat sink is attached is chosen. This is called junction-to-case thermal resistance, $R_{\theta JC}$.

$$R_{\theta JC} = \frac{T_J - T_C}{P_H} \tag{7-2}$$

Where T_C = device case temperature in the steady state test condition [℃]

When the reference point is an ambient temperature, this is called junction-to-ambient thermal resistance, $R_{\theta JA}$.

$$R_{\theta JA} = \frac{T_J - T_A}{P_H} \tag{7-3}$$

Where T_A = Ambient temperature [℃]

$R_{\theta JA}$ (℃/W) indicates the total thermal performance of the SDIP-IPM including the heat sink. Basically $R_{\theta JA}$ is a serial summation of various thermal resistances, $R_{\theta JC}$, $R_{\theta CG}$, $R_{\theta GH}$ and $R_{\theta HA}$.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CG} + R_{\theta GH} + R_{\theta HA} \quad (7\text{-}4)$$

Where, $R_{\theta CG}$ is contact thermal resistance due to the thermal grease between the package and the heat sink, and $R_{\theta GH}$ is heat sink thermal resistance, respectively. From the equation (7-4), it is clear that minimizing $R_{\theta CH}$ and $R_{\theta HA}$ is an essential application factor to maximize the power carrying ability of the device as well as the minimizing of $R_{\theta JC}$ itself. Usually the value of $R_{\theta CH}$ is proportional to the thermal grease and governed by the skill at the assembly site, while $R_{\theta HA}$ can be handled to some extent by selecting an appropriate heat sink.

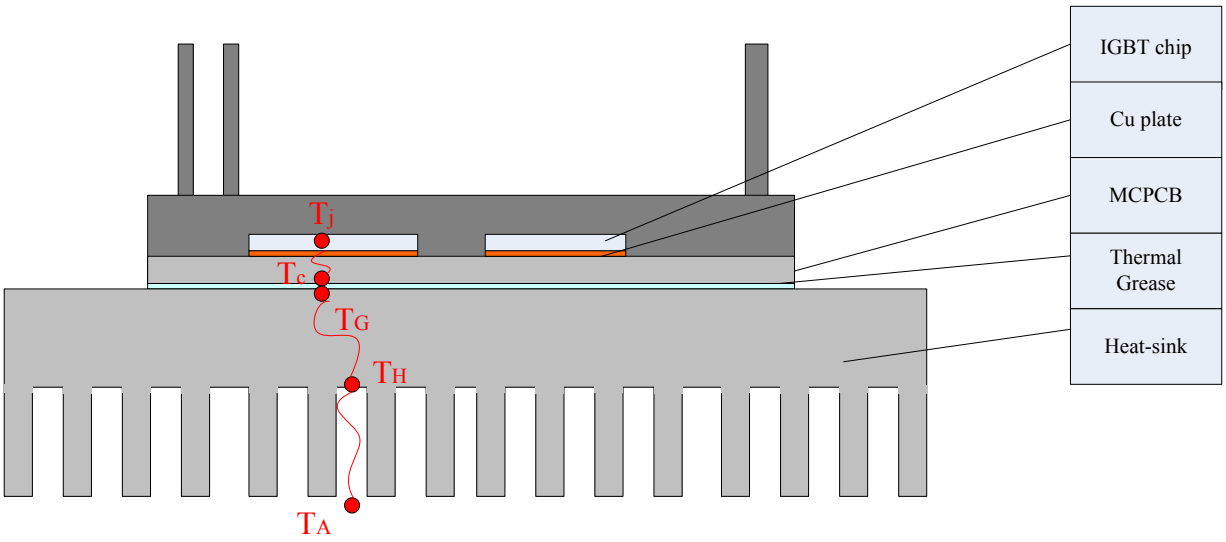


Fig. 7-1 Thermal Network of the ID-IPM from Junction to Ambient

7.2 Measurement Method

During the thermal resistance test, some constants in equation (7-2), i.e., T_C, T_A, and P can be measured directly. The only unknown parameter is the junction temperature, T_J. The Electrical Test Method (ETM) is a popular technique for measuring the junction temperatures in electronic components. However, without a well-defined standard methodology for making thermal measurement, it has become increasingly difficult to accurately determine junction temperature under actual operating and environmental conditions. Knowing the semiconductor device thermal resistance for a specific electronic package allows both the manufacturer and user to determine the junction temperature of the device.

Accurate and correct thermal measurements are difficult to make because of the many variables that impact the final results. Electrical considerations (such as power, voltage and current levels, input and output levels, etc.), environmental considerations (mounting configuration, surroundings, mounting methodology, etc.) and selection of the junction temperature sensor will directly affect the thermal measurement.

The Electrical Test Method (ETM) uses the forward voltage dropped of a junction as the temperature sensitive parameter and is variously known as the “diode-forward-drop” method from original applications with power diodes and bipolar power transistors. It is based on a temperature and voltage dependency exhibited by all semiconductor diode junctions. This relationship can be measured and used to compute the semiconductor junction temperatures in response to power dissipation in the junction region. The voltage-temperature relationships are an intrinsic electro-thermal property of semiconductor junctions, and are characterized by a nearly linear relationship between forward-biased voltage drop and junction temperature when a constant forward-biased current is applied. This constant current is called the “sense current” (also “measurement current”). This voltage drop of the junction is called Temperature sensitive Parameter (TSP). Figure 7-2 illustrates the concept of measuring this voltage versus junction temperature relationship in for a diode junction. The device under test (DUT) is embedded in hot fluid to heat DUT up to desired temperatures.

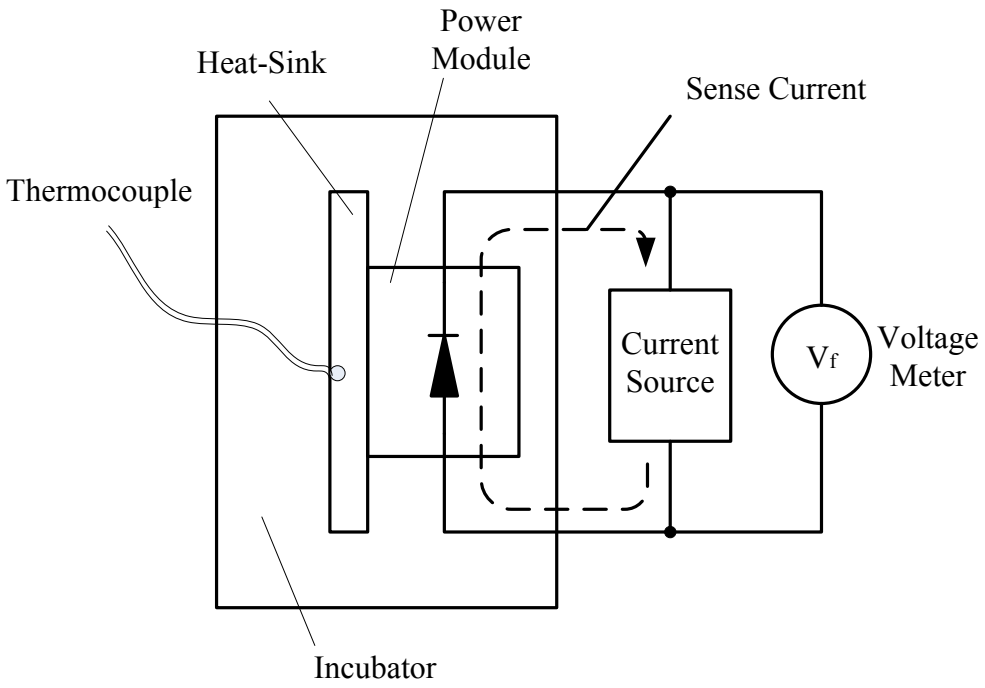


Fig. 7-2 Illustrations of the Bath Method for TSP Measurement

When the DUT attains thermal equilibrium with the hot fluid, a sense current is applied to the junction. Then the voltage drop across the junction is measured as a function of the junction temperatures. The measurement current through the temperature sensing diode must be large enough to obtain a reliable forward voltage reading not influenced by surface leakage effects but small enough not to cause significant self heating. For instance, 1mA, 10mA depending on the device type. The measurements are repeated over a specific temperature range with some specified temperature steps. Figure 7-3 shows a graph of typical result.

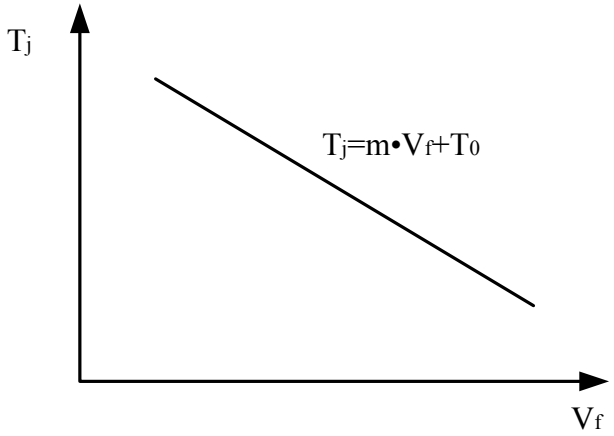


Figure 7-3. Typical Example of a TSP Plot with Constant Sense Current

The relationship between the junction temperature and voltage drop can be expressed mathematically as in the calibrating relationship,

$$T_J = m * V_f + T_0 \tag{7-5}$$

The slope, “m” (deg C/volt) and the temperature ordinate-intercept, “T_0” are used to quantify this straight line relationship. The reciprocal of the slop is often referred as the “K factor” expressed in units of mV/℃. In this case, V_f is the “temperature sensitive parameter” (TSP). For semiconductor junctions, the temperature/voltage slope of the calibrating straight line is always negative, i.e., the forward conduction voltage decreases with increasing junction temperature. Once the slope and intercept have been determined, the junction is calibrated for use as a temperature sensor. The voltage generated in response to the applied sense current can then be used to compute the junction temperature using the calibrating relationship (Equation 7-5).

7.3 Measurement Procedures

This section covers the application of the electrical test method to a variety of functional device categories. These categories are determined by the electrical design of the die utilized in the specific component under test.

Thermal Test Die

Thermal test dice are specifically designed for thermal characterization of integrated circuit packages. These dice are available in a variety of sizes and can be mounted into any desired package to create a thermal test vehicle. They have been designed to offer electrically independent power dissipation and electrical measurement of junction temperature. The thermal die test method is illustrated schematically in figure 7-4. Thermal dice offer accurate thermal characterization with a minimum of measurement hardware. The sense diode voltage can be directly measured with a voltmeter and the associated junction temperature computed (Equation 7-5) using predetermined

calibrating parameters.

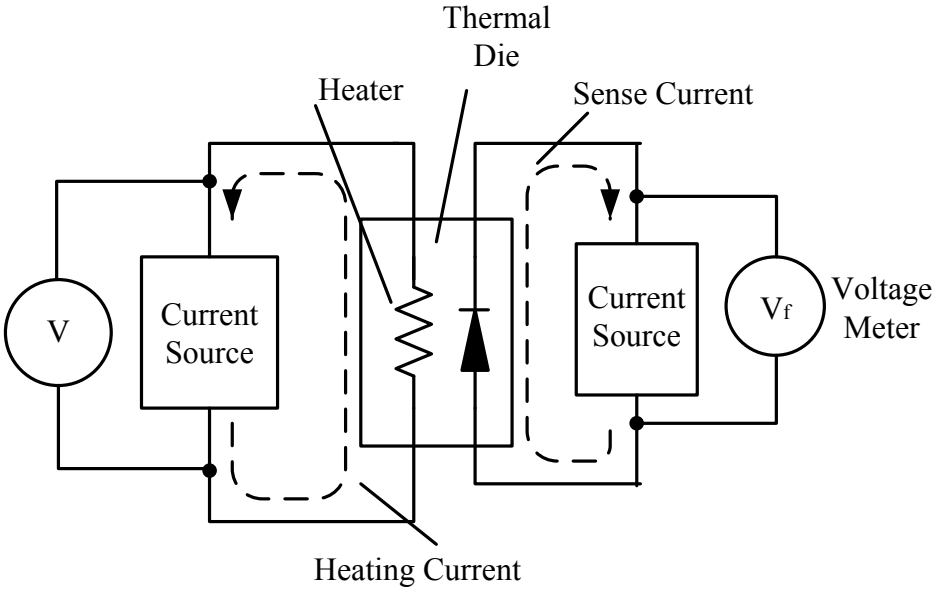


Fig. 7-4 Illustration of Thermal Test Die Test Method Concept

Active Dice

Active or functional dice are often used as the ultimate test for component thermal characterization. The primary feature that distinguishes active die from thermal die is that heat dissipation is not electrically independent from temperature sensing and that the die is designed to perform an electrical function than providing convenient junction temperature reporting. This requires that the otherwise continuous heating power be interrupted for the measurement of the junction temperature. The process of periodically interrupting the heating power to measure the sense junction voltage is best presented with some standard definitions.

The thermal resistance test begins by applying a continuous power of known voltage to the DUT. The continuous power heats up the DUT to a thermal equipment state. The heating interval is the period of time when the heating power is being delivered to the component under test. Active dice are tested with a succession of heating intervals and temperature sampling intervals. During thermal resistance testing, the heating intervals are much longer than the temperature sampling intervals; the heating duty-cycle approaches 100%, which for all practical purposes is considered to be continuous power. Temperature sampling interval is the period of time when the heating power has been interrupted and the sense current has been applied to the sensed junction. The temperature sensitive voltage is measured during this interval. It must be very short so as not to allow for any appreciable cooling of the junction prior to re-applying power. Figure 7-5 illustrates the heating and measurement intervals.

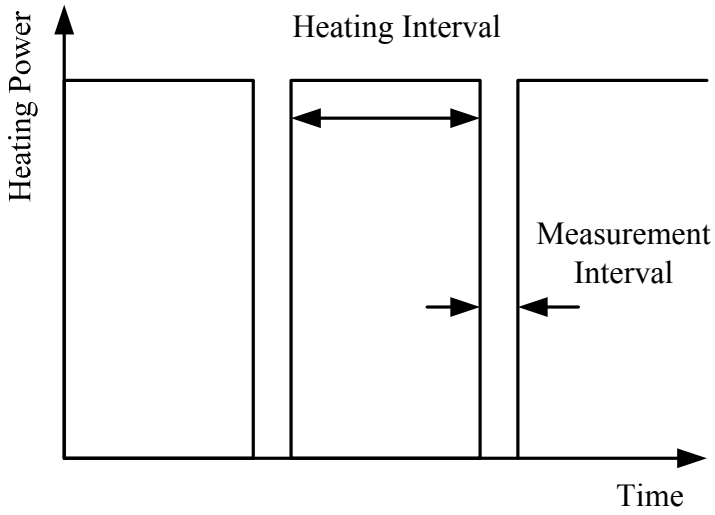
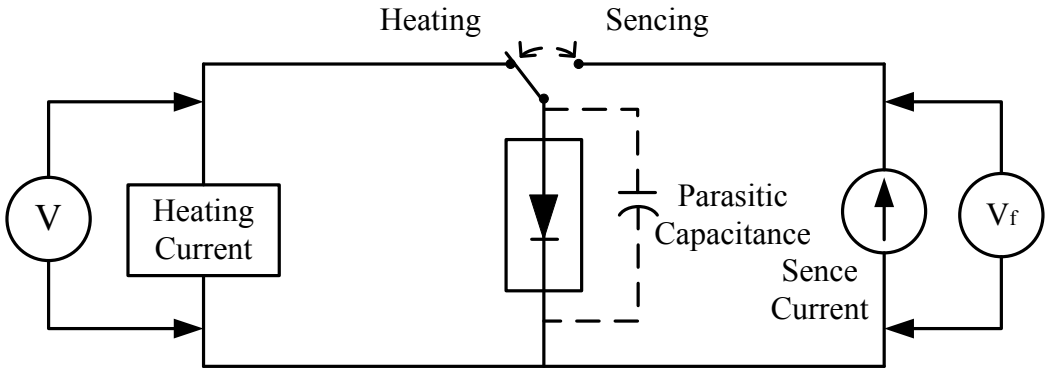


Fig. 7-5 Graphic of Illustration of the Heating and Measurement Intervals

The test procedure for testing a rectifier diode provides an excellent example of some common issues associated with application of the electrical method to active die testing. Figure 7-6 schematically illustrates the electrical test method for a rectifier diode.



$$T_j = m * V_f + T_0$$

$$R_{jx} = (T_j - T_x) / (V * I)$$

Fig. 7-6 Illustration of Diode Test Method Concept

Once T_J reaches thermal equilibrium, its value along with the reference temperature T_C and applied power P is recorded. Using the measured values and equation (7-2), the junction-to-case thermal resistance $R_{\theta JC}$ can be estimated.

Figure 7-7 shows the thermal resistance measurement environment of ID-IPM. The ID-IPM is placed on a heat sink having a large heat carrying capacity. Thermal grease is applied between the ID-IPM and heat sink to prevent an air gap.

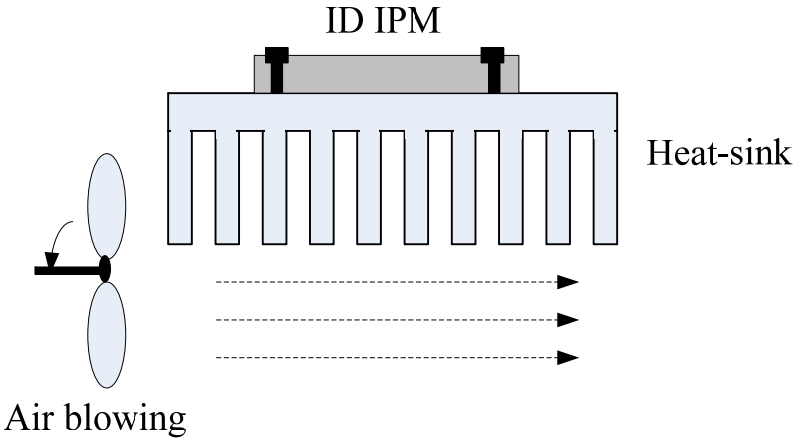


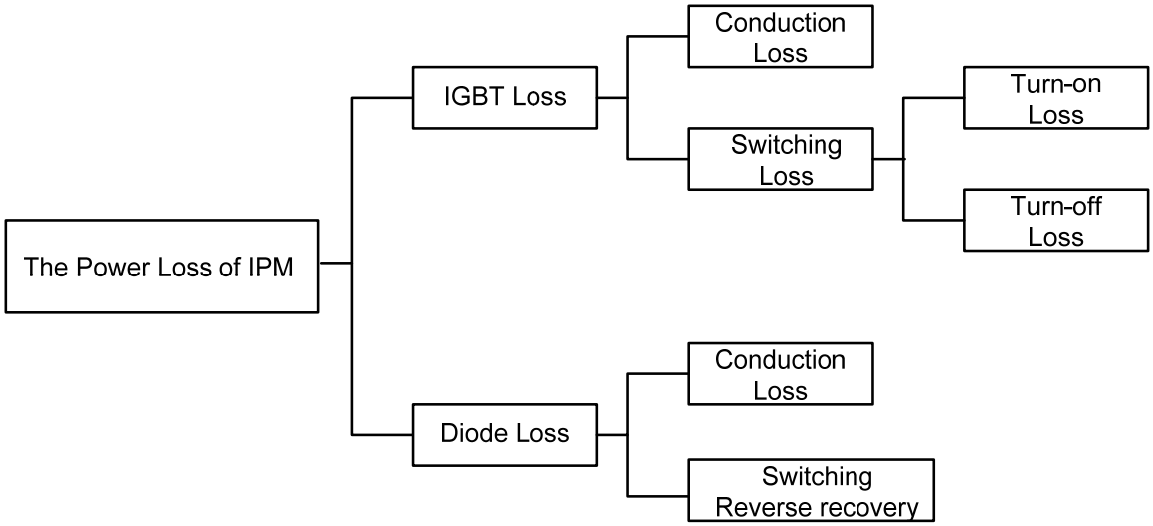
Fig. 7-7 Thermal Measurement Environment of ID-IPM

A thermocouple is inserted through the heat sink and pressed against the underside of the ID-IPM to record the ID-IPM surface temperature. The thermocouple location that the reference temperature (T_C here) needs to be measured, it is recommended that the ideal location is the hottest point.

The thermocouple needs to make a good thermal contact with its reference location. Thermal grease and appropriate clamping pressure are needed.

Chapter 8 Power Loss and Dissipation

An IPM consists of Driver IC, IGBTs and Diodes .The sum of the power losses form these section equals the total power loss for the IPM. The total power losses in the IPM are composed of conduction and switching losses caused in the IGBTs and FRDs. A diagram of the power loss factor is shown as below.



In order to obtain the accurate switching loss, we should consider the DC-link voltage of the IPM system, the applied switching frequency and the power circuit layout in addition to the current and temperature. In this chapter, use these power loss calculations in order to design enough cooling to keep the junction temperature T_j below maximum rated value. Therefore two most important sources of power dissipation that must be considered are conduction losses and switching losses.

8.1 Conduction Loss and Calculation Method

The conduction loss from the IGBT and Diode section can be calculated using the electrical characteristics. The total power dissipation during conduction is estimated by multiplying the saturation voltage by the conducting current. In PWM applications the conduction loss should be multiplied by the duty factor to obtain the average power dissipated. Estimate of conduction losses can be obtained by multiplying the IGBT's rated $V_{ce(sat)}$ by the intended average device current. Actual losses will be less because Vce(sat) is lower value by different rated IC. Free-wheel diodes losses can be estimated by multiplying the forward voltage V_F by intended average diode current.

The most common application of IPMs is the variable voltage variable frequency (VVVF) inverter. In VVVF inverters, PWM modulation is used to synthesize sinusoidal output currents. Figure 8-1 is a typical VVVF inverter current value and operation keep changing .in the active applicatio ID-Series IPM Application Notently changing making loss estimation very difficult. Actual losses will depend on temperature, output current ripple, sinusoidal output frequency and other factors. However, since computer simulations are very complicated, the following is an explanation of a simple method that generates approximate values.

Prerequisites:

For approximate power loss calculations, the following prerequisites are necessary

1. Sine waveform current output PWM control VVVF inverter
2. PWM signals based on the comparison of sine waveform and triangular waveform
3. Three-phase PWM control VVVF inverter for sine-wave current output
4. Output current in ideal sin-waveform
5. The typical forward characteristics are approximated by the following linear equation for the IGBT and the Diode

   $V_{ce(sat)} = V_o + R_i \times i_c$

   $V_F = V_D + R_d \times i_F$

   V_o = Threshold voltage of IGBT V_D = Threshold voltage of diode

   R_i= on-state slope resistance of IGBT R_D = on-state slope resistance of diode

   Where Vce(sat) and VF are the saturation voltage of IGBT and the saturation voltage of diode, as displayed in figure 8-1 the output characteristics of IGBT and Diode have been approximated based on the data contained in the IPM spec.

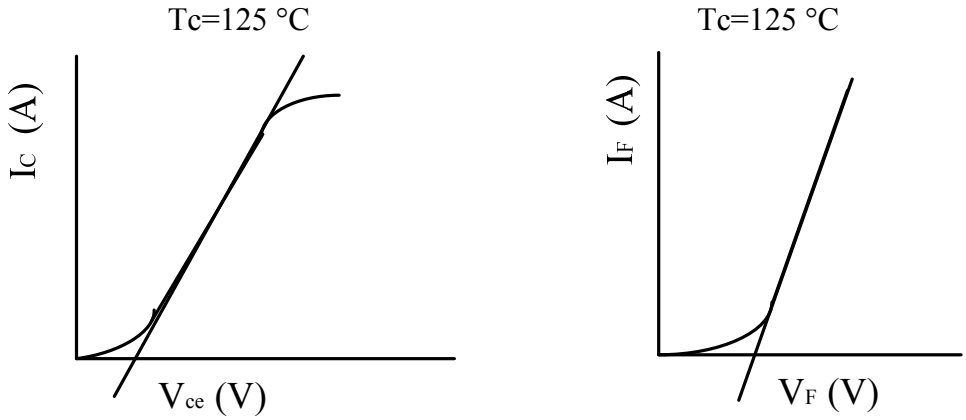


Figure 8-2 Output Characteristics of IGBT and Diode

6. Output current is given by sin x • I_{CP} and it not have ripple current
7. Assume inductive load is ideal and Load power factor for output current is cosθ
8. IGBT saturation voltage Vce(sat) is in proportion to the collector current IC
9. Diode forward voltage drop V_F is in proportion to the forward current Irr

The conduction loss in IGBT and FWD can be calculated as follows:

$$P_{IGBT} = \frac{1}{2} DT \left[\frac{2\sqrt{2}}{\pi} I_M V_O + I_M^2 R \right]$$

$$P_{Diode} = \frac{1}{2} DF \left[\frac{2\sqrt{2}}{\pi} I_M V_D + I_M^2 R \right]$$

DT, DF: Average conductivity of the IGBT and Diode at a half wave of the output current.

8.2 Switching Loss and Calculation Method

Switching loss can be calculated form turn on/off time and over-voltage / current characteristics.
In high frequency PWM switching losses can be extensive and must be considered in thermal design.
The most common method of determining switching losses is to plot the IC and Vce waveforms during the switching transition .Figure 8-3 shown is typical of hard switched inductive load application ex. motor driving application.

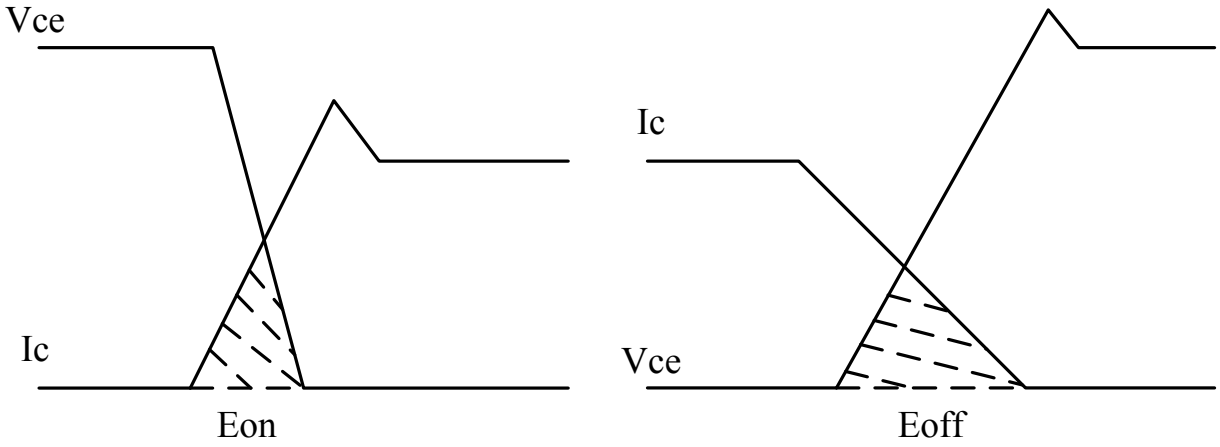


Figure 8-2 Switching Loss

The instantaneous junction temperature rise due to these signals is abnormally overlay and extremely short duration, on the other hand, the sum of these power losses in an application where the device is repetitively switching on and off can be significant. However, different devices have different switching characteristics and they also vary according to the voltage/current and the operating temperature/ frequency. so switching loss energy can be experimentally measured indirectly by multiplying the current and voltage .Therefore the average switching power loss can be calculated by taking the sum of Eon and Eoff and dividing by the switching period T. below is basic equation for average switching power loss:

$$P_{SW(IGBT)} = (E_{ON} + E_{OFF}) \times I \times F_c$$

Where： Fc = Switching Frequency
Eon = Turn-on Switching Energy
Eoff = Turn-off Switching Energy

Figure 8-3 shown is typical of dynamic loss in the Diode can be approximated assuming the idealized waveform .Graphical integration of this waveform yields.

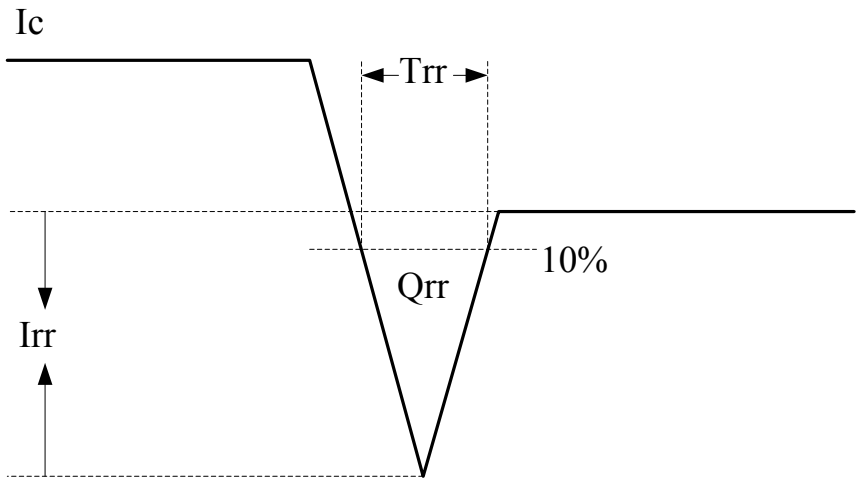


Figure 8-3 Diode loss

Therefore, the loss of diode is idealized as shown in Figure 8-3 and recovery occurs in the middle of output current period. Therefore the formula is below:

$$P_{SW(Diode)} = \frac{1}{2} \times f_c \times \frac{I_{rr} \times t_{rr} \times V_D}{4}$$

IGBT power loss = $P_{IGBT} + P_{SW(IGBT)}$

Diode power loss = $P_{Diode} + P_{SW(Diode)}$

Chapter 9 Appendix Document

9.1 F.A.Q for Starpower ID IPM

1) Circuitry reference design for application

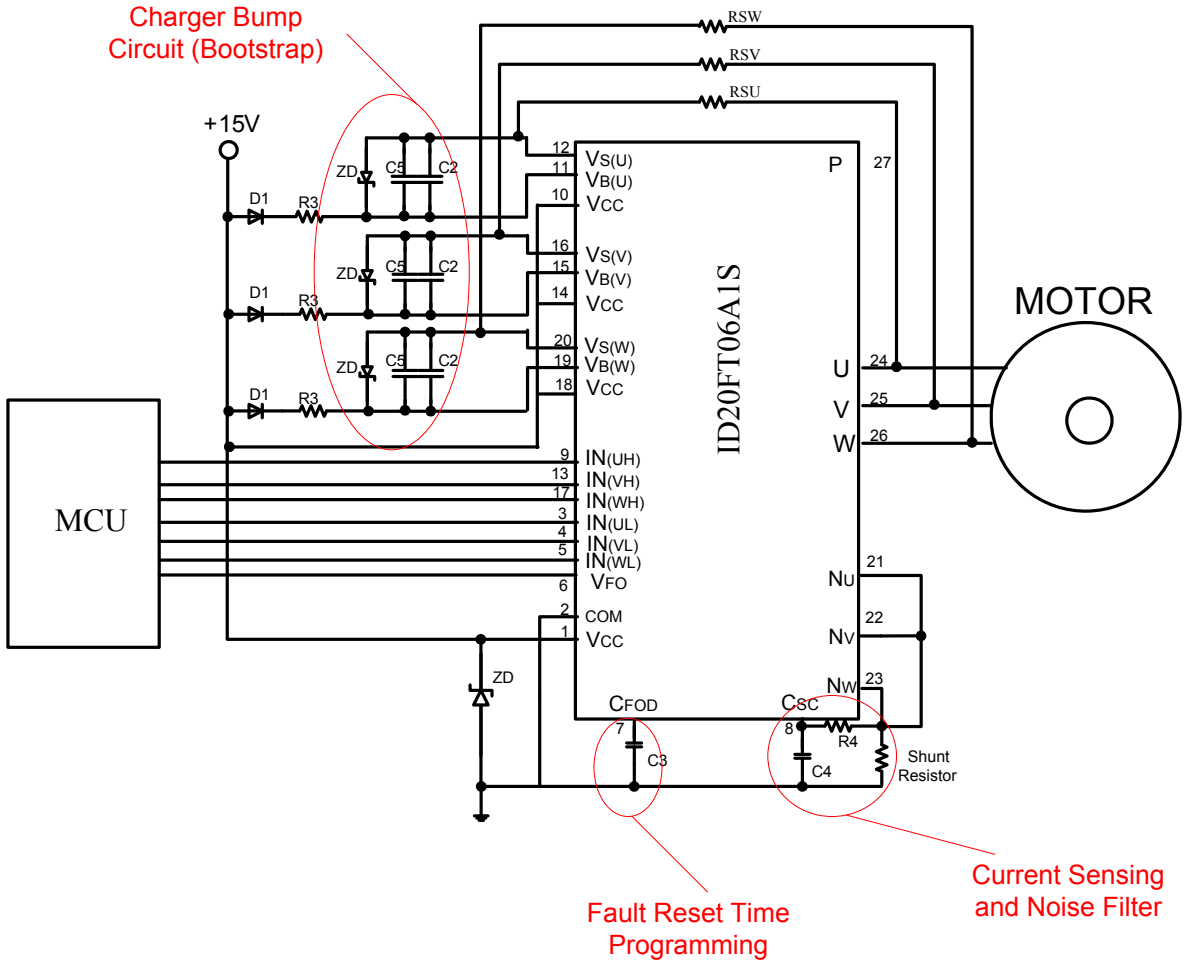


Figure 9-1. Application Circuit

2) Can not start up the system after adopt IPM, or system shut-off immediately after start up.

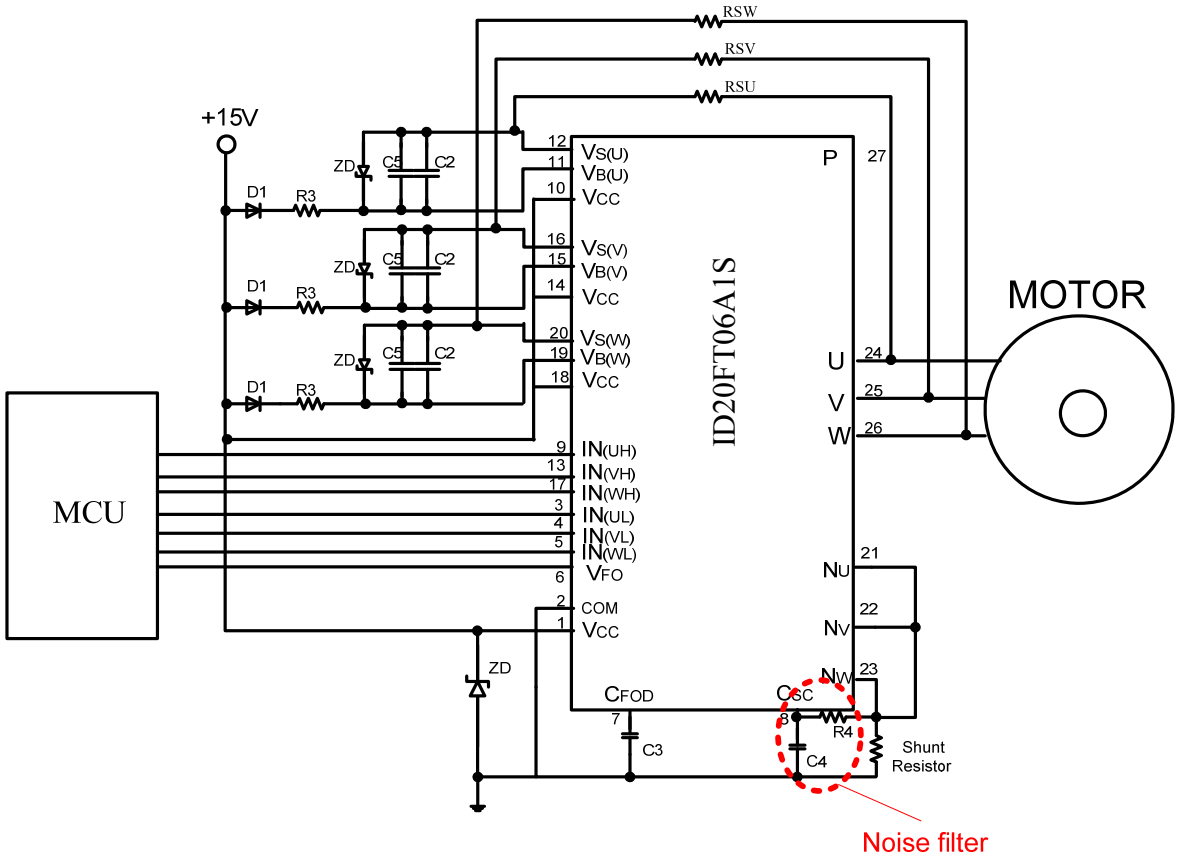


Figure 9-2. Noise Filter Circuit

Possible Answer：Filter in front of the C_{SC} pin is not well designed.
RC circuit should be close to the C_{SC} and COM pin.

3) MCU can not accept the fault signal from IPM for over loading testing.

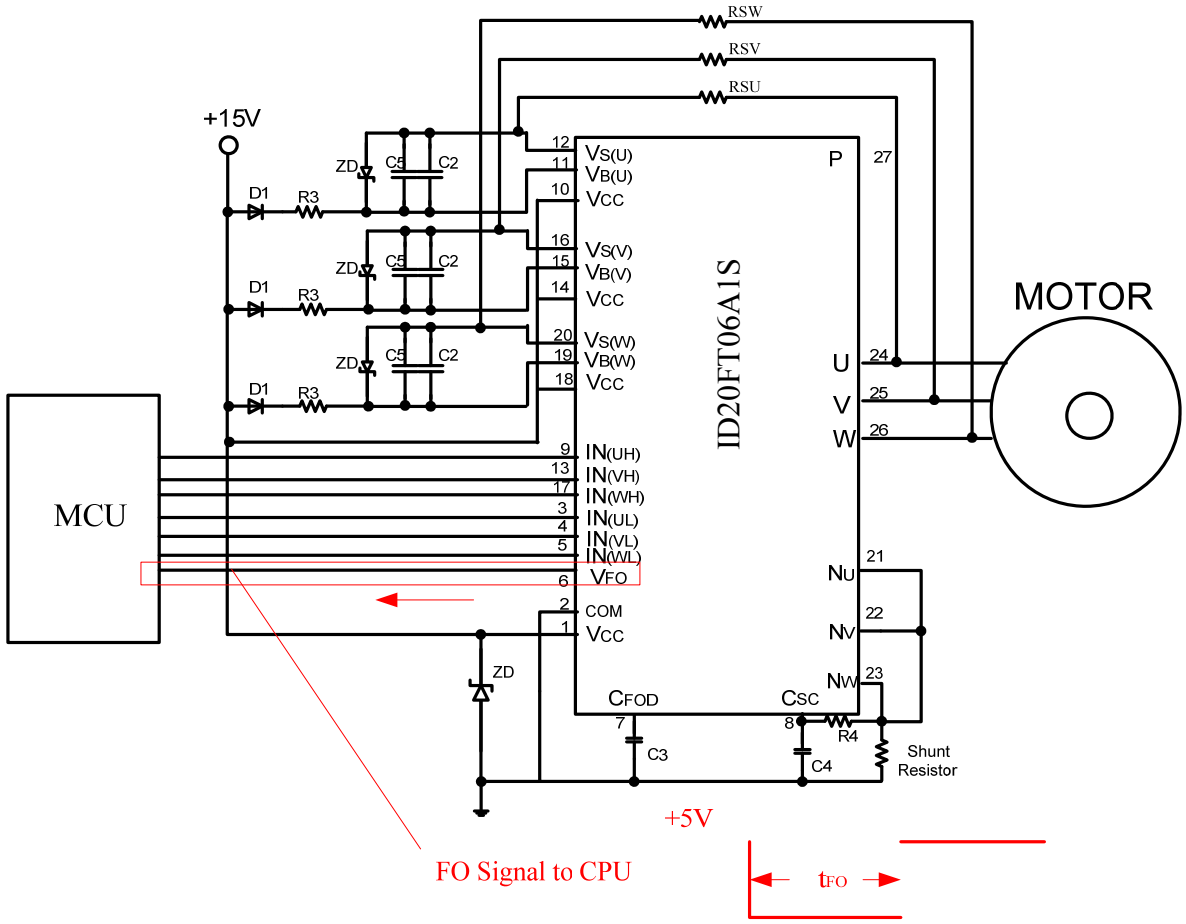
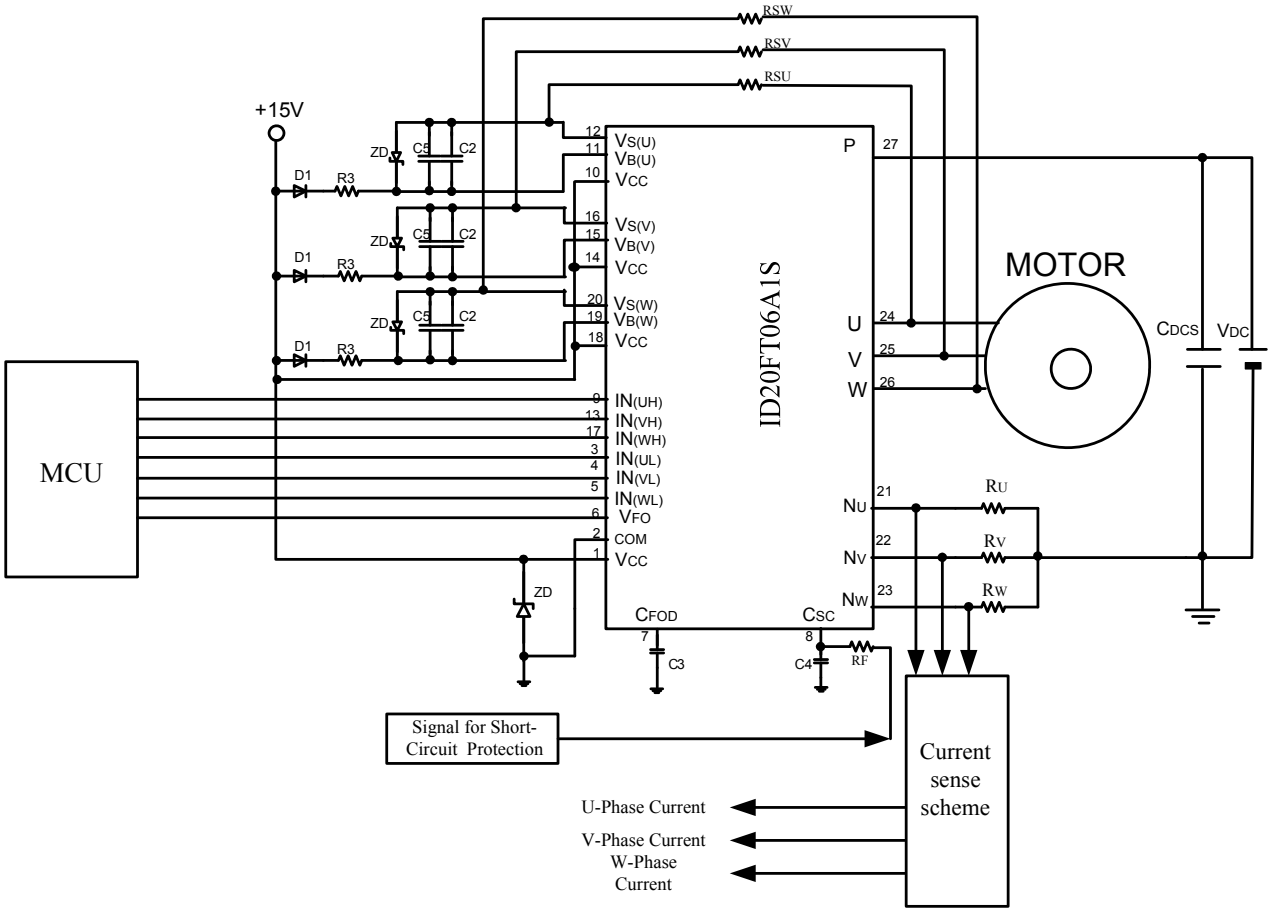


Figure 9-3. FO Signal Circuit

Possible Answer：Pull low period is not long enough to recognize by MCU or not active.

9.2 Divided negative dc-link terminals for current sensing applications



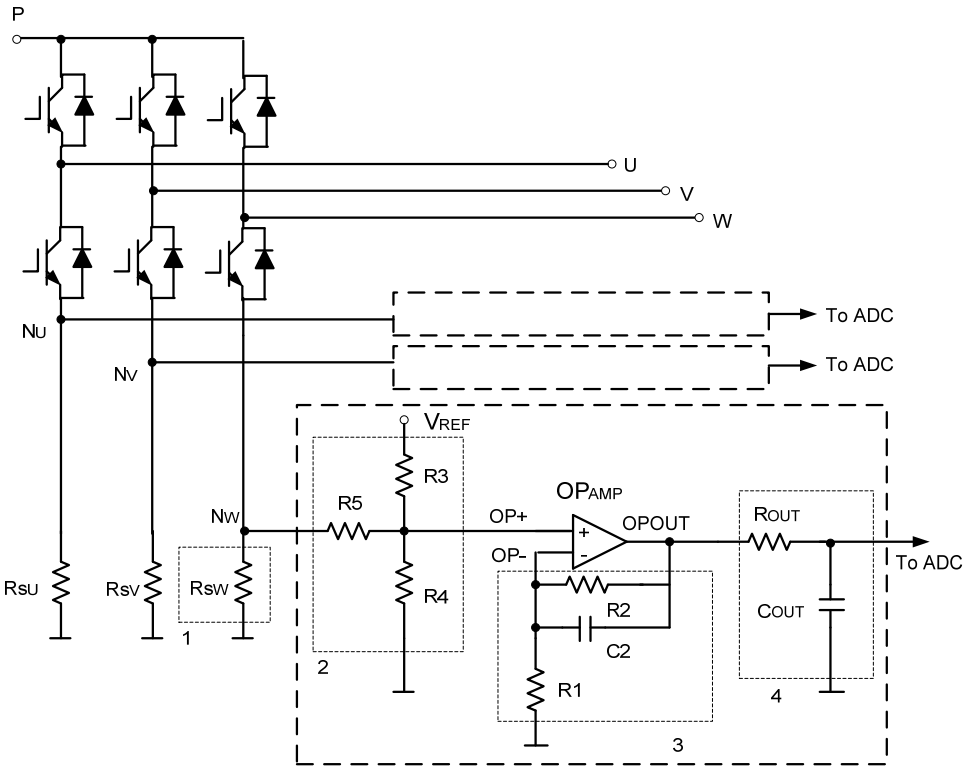


Figure 9-4. Negative DC-link Terminals for Current Sensing Application Circuit

9.3 IPM selection example

- Power factor for most of the motor：0.6 ~ 0.95
- Input power transference efficiency for most of motor：0.7 ~ 0.95

Assume the power factor is 0.9 and efficiency is 80% for the motor you choose, then the current rating for IPM is：

1) Input power is needed for 1HP motor：746W × 1.5 / 0.9 / 0.85 = 1463 VA
2) Three phase inverter output current demand：1463VA / (220V $\times\sqrt{3}$) = 3.84A –Line current
3) Assume the current sharing for power IGBT & Diode is 7：3 by SPWM control.
   (Switching pattern and switching frequency will decide the current sharing)
4) Assume the current sharing for power IGBT & Diode is 1：1 by six-step wave control.
5) Over load capability for acceleration 120% ~300% depends on different application.
6) 3.84 A × 0.7 × 300% = 8.06 A , take 80% as design margin ~ 10A
   ---------- ID15FT06A1S (reference 0.75KW)
7) 3.84 A × 0.5 × 150% = 2.85 A, take 80% as design margin ~ 5A
   ---------- ID10FT06A1S (reference 0.25KW)

IPM selection reference：

Part Number	IGBT Ratings	General Applications		Remark
		PWM Frequency(Typ.)	Motor Ratings(*)	
ID10FT06A1-S	600V/10A	15kHz	0.5 KW/220Vac	V_{iso} = AC 2500V_{rms} (Sinusoidal 1min)
ID15FT06A1-S	600V/15A	15kHz	0.75 KW/220Vac	
ID20FT06A1-S	600V/20A	15kHz	1.5 KW/220Vac	
ID30FT06A1-S	600V/30A	15kHz	2.2 KW/220Vac	

Note：The recommendation table is only for reference, the designer still need to figure out the suitable IPM by more detail calculation.

Chapter 10 Contact Information

We certainly welcome your comments about the application note or any other questions in general.Please feel free to visit our Web site at *http://www.powersemi.cc*

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