Frequently Asked Questions on AESAs and Highly-Integrated Silicon ICs

What is an AESA?

An AESA is an Active Electronically Scanned Antenna, also known as a phased array antenna. As defined by Robert Mailloux, in his *Phased Array Antenna Handbook* (Second Edition, 2005 Artech House), "*phased array antennas consist of multiple stationary elements, which are fed coherently and use variable phase or time delay control at each element to scan a beam to given angles in space.*" Thus, we have electronically-steered beams with no moving parts.

Are AESAs new?

AESAs are not new – they have been built for more than 50 years, but almost exclusively for aerospace and defense applications

Why are AESAs desirable?

AESAs are desirable because they are highly reliable, with no moving parts to fail. They have what is referred to as a "soft failure mechanism," meaning that because there are typically many elements in an array, the failure of a few elements typically has little effect on the performance of the AESA as a whole. AESAs can steer beams quite quickly—in microseconds. They can support multiple, simultaneous, independently-steerable beams. With no mechanically gimbaled parts, they are low profile. AESAs are also able to steer nulls, since they have many elements, they have high degrees of freedom to block interferers and jammers. AESAs can also generate precise, radiating aperture patterns.

How are AESAs used?

Traditionally, they have been implemented as brick-style T/R modules, installed orthogonally to the array, typically installed as MMIC/discrete-hybrid assemblies in machined metal housings. These turn out to be expensive, bulky and heavy, and they limit the range of platforms on which they can be deployed.

In contrast, planar solutions have ICs mounted in the same plane, parallel to the array using all surface-mount assembly techniques. This results in a lower-profile

antenna, reduced wind drag and detectability, and the reduced size and weight enables tower mounting and smaller platforms, such as UAVs.

The lower cost is also enabling new applications, such as commercial radar, next generation SATCOM and 5G terminals.

What are array directivity and gain?

Directivity is the measure of how concentrated the antenna gain is in a given direction relative to an isotropic radiator. It follows a 10*log(N) relationship, where N is the number of elements in the array. Gain, however, takes into account directivity as well as ohmic and scan losses.

What is beam squint?

Beam squint is one of the characteristics of using phase shifters to steer beams of an AESA. Phase shifters electrically steer a beam by approximating time delay. The result is that they only steer the beam perfectly at the center frequency; they understeer at the maximum operating frequency, and they oversteer at the minimum operating frequency. Yet phase shifters are preferred over time delay functions, because of the tradeoff between accuracy and circuit size. In fact, phase shifters provide good accuracy for almost all AESA applications, with the exceptions being very wide instantaneous bandwidth applications, such as EW, or for very large arrays.

What is scan loss?

Scan loss is another characteristic of all AESAs. This is the loss of aperture gain as the beam is steered away from the boresight direction, defined as $\Theta=0$. Scan loss follows $10*\log(\cos^N(\Theta))$ power where Θ is the scan angle and N is a numeric value, typically in the 1.3 range, which accounts for the non-ideal isotropic behavior of embedded element gain.

What is tapering?

Tapering is the process of assigning different gains to the various elements within the array, where the center elements are assigned the highest gains, and the outer elements are assigned lower gains. This is why beam forming typically includes

amplitude control per element, not just phase control. If all elements are treated with the same gain, it is called "uniform illumination." Uniform illumination results in -13 dBc first side lobe levels, which may be unacceptable for some applications due to regulatory, interference or stealth reasons. So gain control allows the AESA system engineer to adjust the gain per element to achieve the desired lower side lobe levels.

Is there a downside to tapering?

Taper can be a good thing, but it does come at a price. The directivity is less than uniform illumination for the same size array, and the beam widths are broader.

What are grating lobes?

Grating lobes are another characteristic of AESAs. They are primarily affected by lattice spacing—the spacing between elements.

What is the traditional AESA construction?

In a traditional AESA construction, the antenna consisted of a number of circuit cards installed orthogonally to the antenna array, each of which feeds a row of radiating antenna elements. These are fed in-turn by individual T/R (transmit/receive) modules, mounted in the plane behind the circuit cards. The large size of the T/R modules means it is difficult to easily reduce the size of the AESA.

How does a planar solution differ from traditional AESA construction?

In a planar solution, the radiating antenna elements are placed on one side of the circuit board, and all of the beam forming electronics are mounted on the reverse side of the panel between the antenna elements. This means the aperture will actually be low profile, which makes handling the array much simpler and much more flexible in how and where the antenna can be mounted.

Where does Silicon come into the AESA picture?

The traditional approach requires a separate T/R module for every radiating element in the array. This means typically that at a minimum, there would need to be a discrete LNA, a PA or driver amplifier, plus control components for each and

every element. Trying to design a planar solution using this approach results in a situation where the required components simply do not fit in the allowable space. And as the frequency increases and the spacing between antenna elements gets smaller, the problem just gets worse.

The obvious solution to this problem is to integrate more functions into a single IC, which reduces the number of required parts. The optimal amount of integration is debatable, but it's clear that if all of the required beam forming circuitry could be included in a single IC, then the floor-planning problems would become significantly easier. But if every element needs all of these components, that means dense integration. And the ability of III-V technologies to do this becomes more challenging. Silicon, though, with its small feature size and multiple metal layers, becomes a more viable candidate as a solution to this problem.

In those applications where high conducted power is needed, then the array can be realized using a common silicon beamforming chip, and a minimal III-V front end, whether that's GaAs or GaN. And the crux of being able to do this is the ability to integrate all the required beamforming circuitry within a single IC.

How is performance impacted by the increased integration?

With increased integration and compaction, there is some resulting degradation in performance. The area of greatest concern for the beamformer is the ability to maintain adequate isolation between the independent channels. Unwanted coupling paths between the channels could either be on the board, in the package or package transitions, or through signal paths on the IC itself.

Regardless of the source of the coupling, the effective degradation to the channel-to-channel isolation is the same. A random error vector is introduced and superimposed onto the designed phasor, resulting in a corruption of the desired signal. The net effect of this is to limit the accuracy available from the vector modulator and therefore place an upper limit on the resolution of the number of bits that can be used in the beam steering.

How do the Anokiwave X-Band Silicon Quad Core ICs present a solution?

As an example, the Anokiwave X-Band Silicon Quad Core IC (AWS-0103/AWS-0101) is available in two versions: a high-receive linearity power feed with a III-V front end, and a high-gain, low noise figure version for use in an all-silicon array. The schematic block diagram of both versions is exactly the same. The quad IC supports four radiating elements, four channels on transmit, eight channels on receive, each of which has independent beam steering. There are two common RF beam forming ports, one of which is shared in time-duplex fashion with a transmitter.

When sending a transmit waveform, the signal is input to the common beam port, split two ways, and then split a second time to give us four transmit signals. After passing through the vector modulators, each path is amplified to a level of about +15 dBm, which can be used to either drive a high-power III-V stage or used directly at the elements for an all-silicon array.

In receive mode, we have two independent receive paths providing the ability to either do simultaneous processing of orthogonal linear polarizations, or multiple sample processing of the same receive signal. The receive signal paths are coherently combined in two separate combiners and output from the chip to enable the next level of RF signal combining at either the sub-array or the array level.

In addition, there is a control and telemetry block that supports two-way communication over a digital SPI interface, as well as providing and enabling a set of controls for the RF vector modulators. The telemetry block also outputs diagnostic data from on-chip power detectors and temperature sensors. Power detection at all transmit ports as well as local temperature sensing, is sampled, digitized on-chip and then made available to the host system.

Each vector modulator within the IC used for beam steering can be independently controlled in both amplitude and phase within 6 bits of precision. That means 12 bits per vector modulator: 6 bits amplitude and 6 bits phase and a total of 96 bits for the entire beamformer. Six bits of phase modulation control implies least significant bit of 5.625 degrees. And the six bits of amplitude control uses the least significant bit of 0.5 dB, resulting in almost 32 dB dynamic range of aperture control.

As mentioned previously, amplitude control is useful for an array taper to give added flexibility for control of side lobes for regulator emissions compliance.

What is the cost implication for commercial applications?

Key performance metrics (noise figure, beam steering accuracy, channel-to-channel isolation) are all possible in silicon ICs, even when mounted in low-cost, commercial plastic packages. And this is important, because emerging applications—especially next generation SATCOM and 5G applications—need AESA technology at commercial and consumer price points in order to be successful.