A Highly Integrated Gallium Nitride S-Band Radar Pallet Amplifier

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Abstract:

This paper presents a highly integrated S-Band radar pallet amplifier using GaN technology with a sequencing circuit capable of drain pulse modulation. The design of a 350W S-Band pallet comprised of two packaged GaN on Silicon Carbide hybrid power transistors, impedance matching networks, combining structures and the relevant sequencing and bias circuitry will be described. The 350W pallet amplifier is a 50Ω input and output impedance amplifier operating with a single positive supply.

I. Introduction

High power Gallium Nitride (GaN) RF transistors have well known advantages over current bipolar and LDMOS technology such as superior power density for a given die size, higher frequency of operation, wider bandwidths and higher efficiency. Significantly higher breakdown voltages also results in higher voltage operation, ability to match the device for harmonically terminated high efficiency modes of operation and ruggedness into high load mismatch conditions. As GaN emerges as a key technology being deployed in next generation high power RF amplifier applications such as radar, electronic warfare, military and commercial communications as well as avionics, system designers also need to adapt their implementations to accommodate the differences of GaN transistors technology versus their bipolar and LDMOS predecessors.

The GaN transistors used in this development are depletion mode HEMT (High Electron Mobility Transistors) devices requiring a negative gate voltage be applied prior to the positive drain voltage. Although GaAs transistor amplifier designs employ sequencing circuits as they are also depletion mode transistors, power amplifier designs at S-Band and below utilizing bipolar and LDMOS technology have not needed any such sequenced biasing.

This paper presents a highly integrated S-Band radar pallet amplifier using GaN technology with a sequencing circuit capable of drain pulse modulation. Although this pallet is geared specifically for a radar application, many of the integrated features can be applied to any RF power amplifier applications which utilize gallium nitride power transistors.

II. Pallet Design Overview

The 350W S-Band pallet is comprised of two 180W packaged GaN on Silicon Carbide hybrid power transistors, printed impedance matching networks, combining structures and the relevant sequencing and bias circuitry. Figure 1 shows a block diagram of the integrated pallet. Table 1 shows a list of design objectives. The pallet amplifier is a 50Ω input / output impedance amplifier operating with a single positive supply. Operation of the amplifier is in a Class AB mode allowing for low quiescent current settings as some level of power level control.

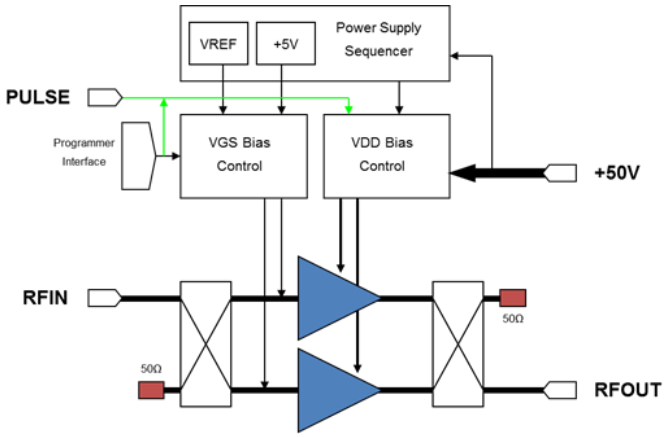

Figure 1: Pallet Amplifier Block Diagram

Parameter	Requirement
Frequency	2.7 – 3.1GHz
Power	350W minimum
Gain	11 dB minimum
Gain Flatness	0.5 dB maximum
Efficiency	40% minimum
Pulse Droop	0.6dB maximum
Size	2.5”(64mm)x1.5”(38mm)
Pulse Blanking	TTL signal
Drain Voltage	50V (single voltage)

Table 1: Pallet Amplifier Design Objectives

III. Bias and Sequencing Circuitry

An on board power supply sequencing circuit manages the order and timing of the gate (VGS) and drain (VDD) bias voltages to ensure safe operation of the GaN devices. Improper sequencing such as applying the +50V drain voltage before the negative gate voltage will quickly lead to catastrophic failure of the GaN device.

The internal +5V regulator provides power to the VGS negative voltage generator and also to the other control circuitry on the hybrid. The VGS voltage is stabilized using a temperature stable voltage reference VREF. These voltage sources are also controlled by the power supply sequencer. During power up, the +50V VDD supply is held off until the gate bias voltage is set and stable. Once VGS is stable, the PULSE control circuitry is enabled to allow the +50V supply to connect to the VDD of each device.

The PULSE control signal is also available to the user as a TTL level input for externally switching the VDD bias on and off. This gives the user the ability to control the average DC power consumed by the hybrid during low duty cycle pulsed operation or to simply switch off the GaN devices in a powered down energy conservation state to maximize system efficiency. This is referred to as blanking and it not only improves efficiency, it eliminates transmit noise power during the receive period by effectively turning the transistors off.

The Power Supply Sequencer will also safely shut down the GaN devices when the +50V supply is turned off or abruptly removed.

A programming interface is provided to adjust the VGS of each GaN device separately and to lock those settings into an on board EEPOT. The integrated pallet bias is factory programmed for optimum performance but the VGS can be field programmed using a custom USB controlled device programmer.

IV. Power Amplifier Design

The power amplifier design portion is a straightforward implementation using a balanced configuration. Identical low loss surface mount 3dB hybrid couplers are used for the divider and combiner. The balanced configuration provides good isolation between both RF transistors which improves stability. Additionally, balanced amplification provides better input and output return loss when compared to a single ended transistor since reflected power is absorbed by the 50Ω load in the decoupled coupler port.

The 180W transistors have internal matching in conjunction with printed external matching optimized for pulsed operation between 2.7 – 3.1 GHz. The transistor design represents an optimal balance between gain, output power, bandwidth, stability and efficiency.

V. Pallet Construction

In designing an integrated amplifier it is essential to understand key size, cost and thermal requirements of the finished pallet. To reduce cost the pallet makes use of a laminated hybrid approach. The RF laminate provides a low loss solution for the distributed matching circuitry while making it possible to use low cost SMT technology for the integration of the RF components and associated control circuitry. The laminate substrate is bonded to a thermally enhanced metal material using conductive epoxy. Both the laminate and the metal carrier in conjunction with the bonding epoxy have been thoroughly tested for robustness on modern lead free reflow environments to ensure no delamination occurs in either the laminate material itself or the between the board and the metal carrier.

VI. Results

Figure 2 shows a picture of the completed pallet.

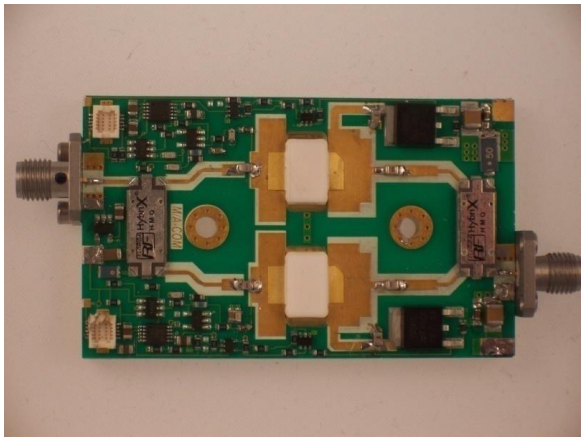

Figure 2: Integrated Pallet Amplifier

The RF performance at 2.9 GHz yielded 11.4 dB of large signal gain with 385W of output power when operated at P2dB. Testing was done with a 300µs pulse at 10% duty cycle. The Class AB quiescent current was set to 400mA per device.

Utilizing the TTL PULSE feature to remove the drain voltage to the transistors between pulses, efficiency was measured at 42% which is 2% higher than keeping the transistors turned on continuously, a further savings of 8W on DC consumption.

The timing response of the pulse blanking feature was also characterized. Figure 3 shows the rise time of the active load TTL PULSE signal, VDD and the detected RF envelope. To safely turn the drain on in advance of the RF pulse, the TTL pulse should lead the RF pulse by 2 µs. Similarly, the PULSE signal should follow the RF pulse by 2 µs. Figure 4 shows the timing of an entire 300 µs pulse.

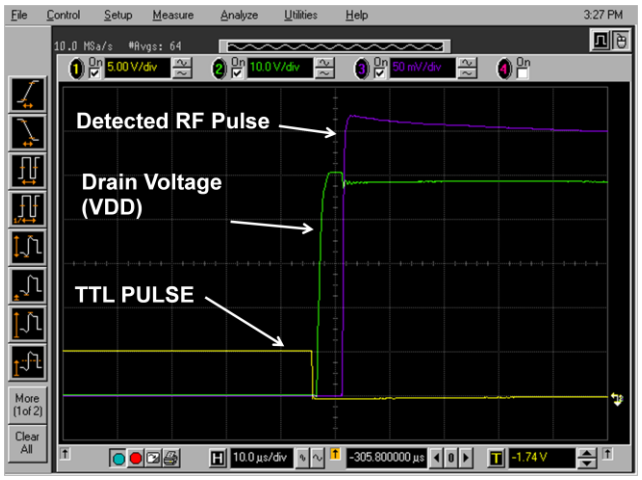

Figure 3: Measured Rise Time Results

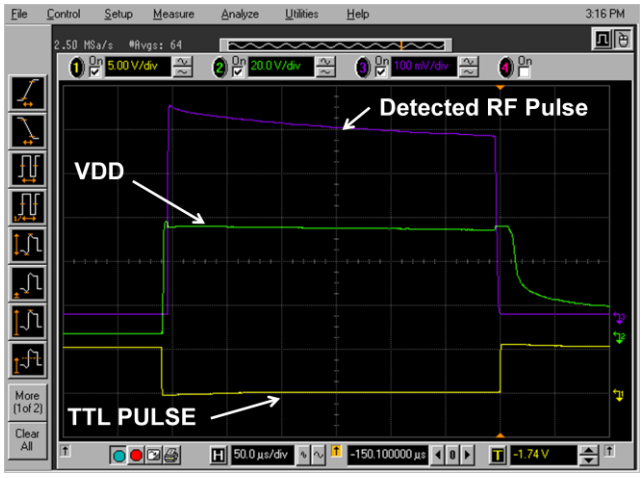

Figure 4: Measured Pulse Results

CONCLUSION

A highly integrated S-Band radar pallet utilizing GaN high power transistors was demonstrated. The design met both the RF and control objectives. The integrated pallet design approach provides the engineer greater flexibility and engineering savings during their system design phase while providing ease of scalability and yield improvements during volume production. The bias control and sequencing circuitry can be used as a building block for future pallet designs.

ACKNOWLEDGEMENT

The author expresses his gratitude to Craig Walsh and Paul Clark of Telemakus for their efforts in the development of this pallet.

AUTHOR BIO

Gregory French is a Business Development Manager at M/A-COM Technology Solutions. He received his bachelor's and master's degree from the University of Massachusetts, Amherst. He has been involved with high power amplifier designs and technology development for military and commercial products throughout his career.