Tecate Group
The power of the future. Today.

Ultracapacitor & Supercapacitor Frequently Asked Questions

What is an ultracapacitor?

Electric double-layer capacitors, also known as supercapacitors, electrochemical double layer capacitors (EDLCs) or ultracapacitors are electrochemical capacitors that have an unusually high energy density when compared to common capacitors, typically several orders of magnitude greater than a high-capacity electrolytic capacitor.

The electric double-layer capacitor effect was first noticed in 1957 by General Electric engineers experimenting with devices using porous carbon electrode. It was believed that the energy was stored in the carbon pores and it exhibited "exceptionally high capacitance", although the mechanism was unknown at that time.

General Electric did not immediately follow up on this work, and the modern version of the devices was eventually developed by researchers at Standard Oil of Ohio in 1966, after they accidentally re-discovered the effect while working on experimental fuel cell designs. Their cell design used two layers of activated charcoal separated by a thin porous insulator, and this basic mechanical design remains the basis of most electric double-layer capacitors to this day. With advances made on both materials and manufacturing process, today Tecate Group PowerBurst® product show a superior advantage amongst all other ultracapacitors in the market.

Generally, capacitors are constructed with a dielectric placed between opposed electrodes, functioning as capacitors by accumulating charges in the dielectric material. In a conventional capacitor, energy is stored by the removal of charge carriers, typically electrons from one metal plate and depositing them on another. This charge separation creates a potential between the two plates, which can be harnessed in an external circuit. The total energy stored in this fashion is a combination of the number of charges stored and the potential between the plates. The former is essentially a function of size and the material properties of the plates, while the latter is limited by the dielectric breakdown between the plates. Various materials can be inserted between the plates to allow higher voltages to be stored, leading to higher energy densities for any given size. For example aluminum electrolytic and tantalum electrolytic capacitors, use an aluminum oxide film and a tantalum oxide film as the dielectric, respectively. In contrast, Electric Double Layer Capacitors do not have any dielectrics in general, but rather utilize the phenomena typically referred to as the electric double layer. In the double layer, the effective thickness of the "dielectric" is exceedingly thin, and because of the porous nature of the carbon the surface area is extremely high, which translates to a very high capacitance. Generally, when two different phases come in contact with each other, positive and negative charges are set in array at the boundary. At every interface an array of charged particles and induced charges exist. This array is known as Electric Double Layer. The high capacitance of an EDLC arises from the charge stored at the interface by changing electric field between anode and cathodes.
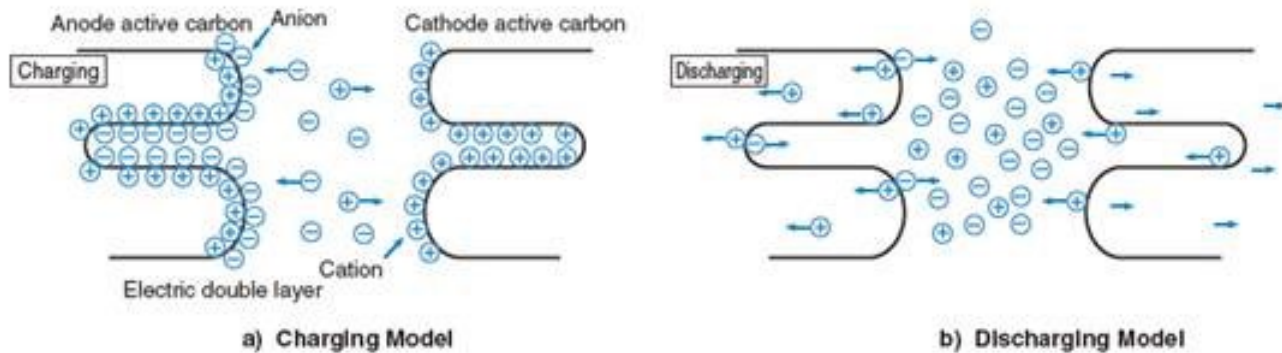
Figure 1: Ultracapacitor Charge Separation

However, the double layer capacitor can only withstand low voltages (typically less than 2.7V per cell), which means that electric double-layer capacitors rated for higher voltages must be made of matched series-connected individual capacitors, much like series-connected cells in higher-voltage batteries.

There are 2 types of electrolytes used by EDLC manufacturers. One is water-soluble and the other is non-water soluble. The non-water soluble electrolyte does increase the withstand voltage per cell compared to that of a water soluble electrolyte, hence producing a higher energy density. Tecate Group PowerBurst® cells are made with non-water soluble electrolytes, and feature a small size and light weight.

What are Ultracapacitors advantages & challenges?

Each application needs to be evaluated based on its requirements. Below are some of the advantages and disadvantages when considering the use of EDLCs:

Advantages:

• High energy storage. Compared to conventional capacitor technologies, EDLCs possesses orders of magnitude higher energy density. This is a result of using a porous activated carbon electrode to achieve a high surface area.

• Low Equivalent Series Resistance (ESR). Compared to batteries, EDLCs have a low internal resistance, hence providing high power density capability.

• Low Temperature performance. Tecate Group PowerBurst® products, with their use of patented technology, are capable of delivering energy down to -40°C with minimal effect on efficiency.

• Fast charge/discharge. Since EDLCs achieve charging and discharging through the absorption and release of ions and coupled with its low ESR, high current charging and discharging is achievable without any damage to the parts.

Disadvantages:

• Low per cell voltage. EDLC cells have a typical voltage of 2.7V. Since, for most applications a higher voltage is needed, the cells have to be connected in series.

• Cannot be used in AC and high frequency circuits. Because of their time constant EDLCs are not suitable for use in AC or high frequency circuits.

The specifics of ultracapacitor construction are dependent on the manufacturer, and the intended application. The materials may also differ slightly between manufacturers or due to specific application requirements. The commonality among all ultracapacitors is that they consist of a positive electrode, a negative electrode, a separator between these two electrodes, and an electrolyte filling the porosities of the two electrodes and separators.
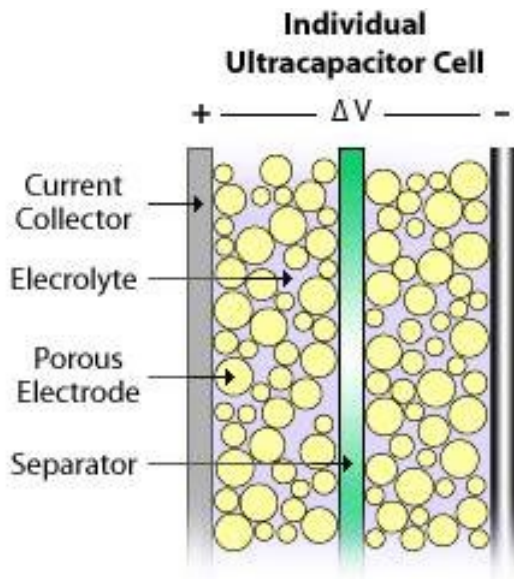

Figure 4: Internal Cell Construction

Today, in general, most manufacturers have adopted a cylindrical construction method for their EDLCs. However, there are still products in the market that use a prismatic design. Each method has its own advantages and disadvantages which may or may not affect their use in specific applications. Tecate's PowerBurst® products use the round or cylindrical construction method. The cells are constructed from activated carbon particles, mixed with a binder and then deposited on aluminum foil. In this method, as shown in the following figure, the electrodes are wound into a jellyroll configuration very similar to an aluminum electrolytic capacitor. The electrodes have foil extensions that are then welded to the terminals to enable a current path to the outside of the capacitor.
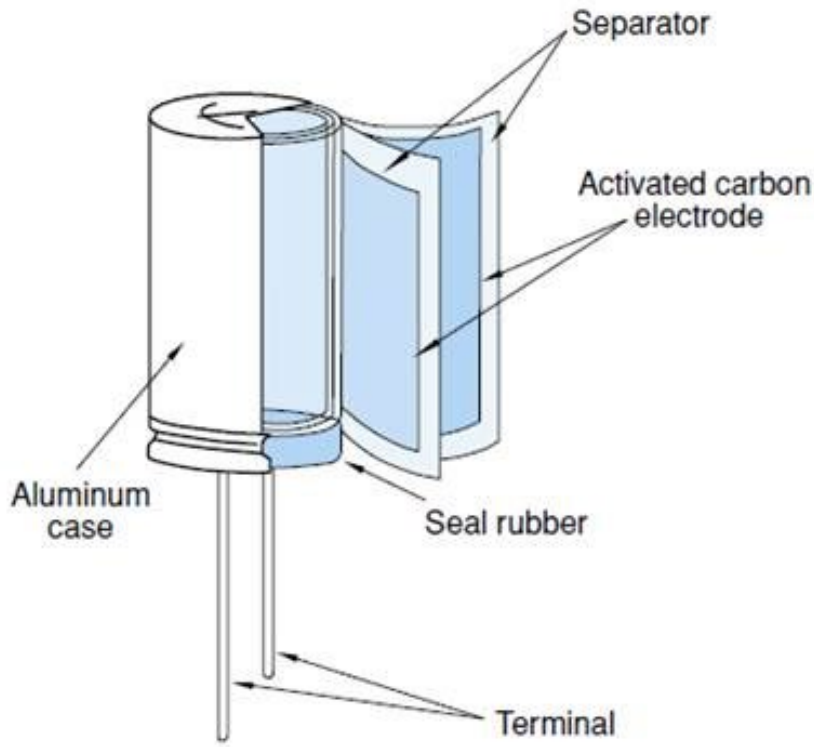
Figure 5: Cell Construction

EDLCs share the same equivalent circuit as conventional capacitors. The first order model is represented by the circuit below. It is comprised of four ideal components. The series resistance Rs which is also referred to as the equivalent series resistance (ESR). This is the main contributor to power loss during charging and discharging of the capacitor. It is also comprised of a parallel resistance Rp which affects the self-discharge, a capacitance C and a series inductor Ls that is normally very small as a result of the cell construction.

Figure 6: First Order Equivalent Circuit

Since Rp is always much larger than Rs it can be ignored. Also, because of the porous material used on the electrode of EDLCs, they exhibit non-ideal behavior which causes the capacitance and resistance to be distributed such that the electrical response mimics transmission line behavior. Therefore, it would be necessary to use a more general circuit, as shown in the figure 6, for representing the real electrical response.
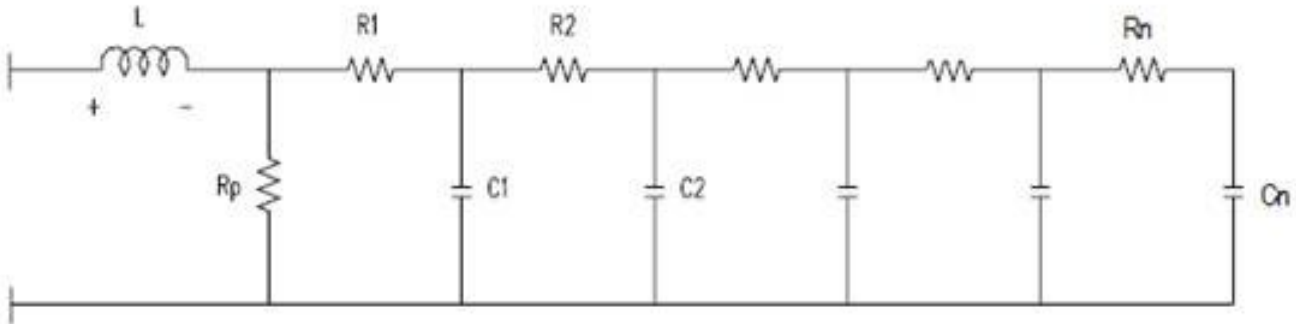

Figure 7: Ladder Network

However, to simplify the circuit we can model the EDLC as an RC circuit. In this case the charge stored is Q=CV. The energy stored in the capacitor in Joules (watt-second) = 1/2CV2. Other useful formulas are discussed more in the sizing section.

One final note to consider in regards to EDLC, is the discharge characteristics of the cells. Unlike batteries which can discharge a fairly constant voltage, the EDLC cells act very similar to traditional capacitors and will drop their voltage as they discharge their stored energy similar to what is shown in Figure 8.
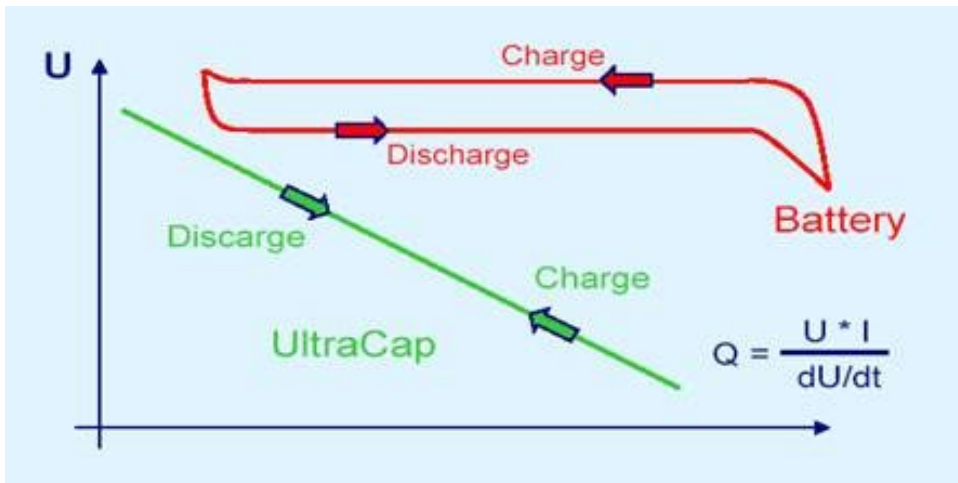

Figure 8: Ultracapacitor Discharge Curve

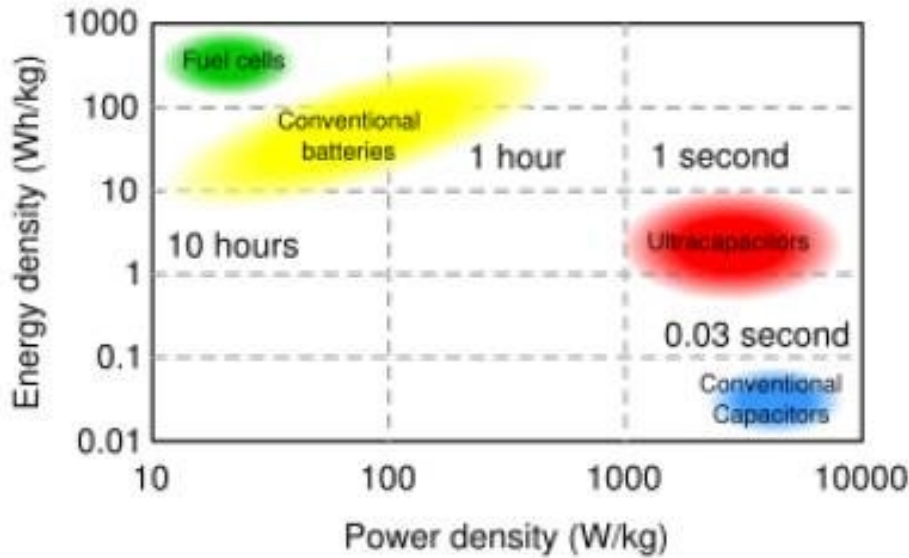# How Do Ultracapacitors Differ From Battery And Traditional Capacitors?

Figure 2: Ragone Plot

As can be seen in Figure 2, the Ultracapacitors reside in between conventional batteries and conventional capacitors. They are typically used in applications where batteries have a short fall when it comes to high power and life, and conventional capacitors cannot be used because of a lack of energy. EDLCs offer a high power density along with adequate energy density for most short term high power applications. Many users compare EDLCs with other energy storage devices including batteries and conventional capacitor technology. Each product has its own advantages and disadvantages compared to other technologies as can be seen from the chart below:

Available Performance	Lead Acid Battery	Ultracapacitor	Conventional Capacitor
Charge Time	1 to 5 hrs	0.3 to 30 s	10^{-3} to 10^{-6} s
Discharge Time	0.3 to 3 hrs	0.3 to 30 s	10^{-3} to 10^{-6} s
Energy (Wh/kg)	10 to 100	1 to 10	< 0.1
Cycle Life	1,000	>500,000	>500,000
Specific Power (W/kg)	<1000	<10,000	<100,000
Charge/discharge efficiency	0.7 to 0.85	0.85 to 0.98	>0.95
Operating Temperature	-20 to 100 C	-40 to 65 C	-20 to 65 C

Figure 3: Ultracapacitors vs. Battery and Conventional Capacitors

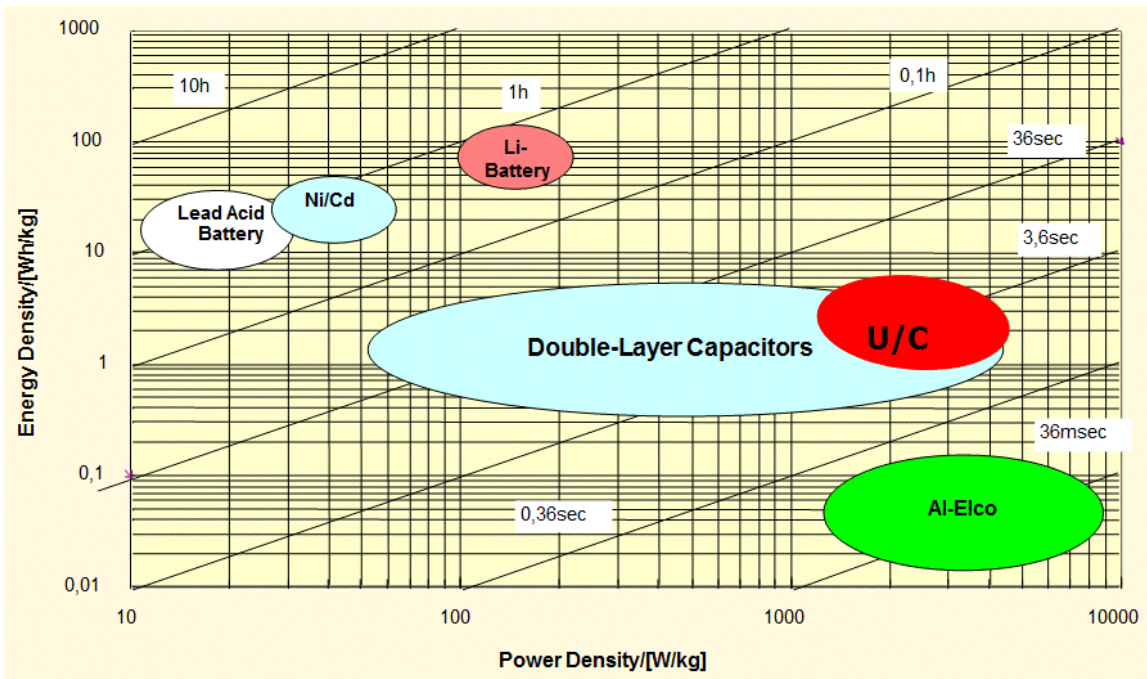![Tecate Group - The power of the future. Today.]

What Is The Difference Between Power And Energy?

Power * Time = Energy
Power is the rate of using energy.


Power Density vs Energy Density

What Are The Key Applications For Ultracapacitors?

- Ultracapacitor Functions
    - Secure power
        - Provides reliable interim power, even if the primary source fails or fluctuates
    - Energy storage
        - Stores energy from low power sources, enabling support for high power loads
    - Pulse power
        - Supplies peak power to the load while drawing average power from the source
- User Benefits
    - Reduces the size & weight of the battery / power source required
    - Improves run-time & battery life, particularly at cold temperatures
    - Enables more power-hungry features, being used more often
    - Can remove the need for a battery & harvest energy from clean sources
    - Protects against accidental power loss or fluctuations/interruptions
    - Doesn't need to be replaced like batteries (unlimited discharge cycles)
    - Environmentally friendly & safe

What Is End Of Life And Failure Mode For An Ultracapacitor?

In general ultracapacitors do not have a hard end of life failure similar to batteries. Their end of life is defined as when the capacitance and/or ESR has degraded beyond the application needs.

Cap failure under typical use condition

Capacitance Change@ 65C/2.7V
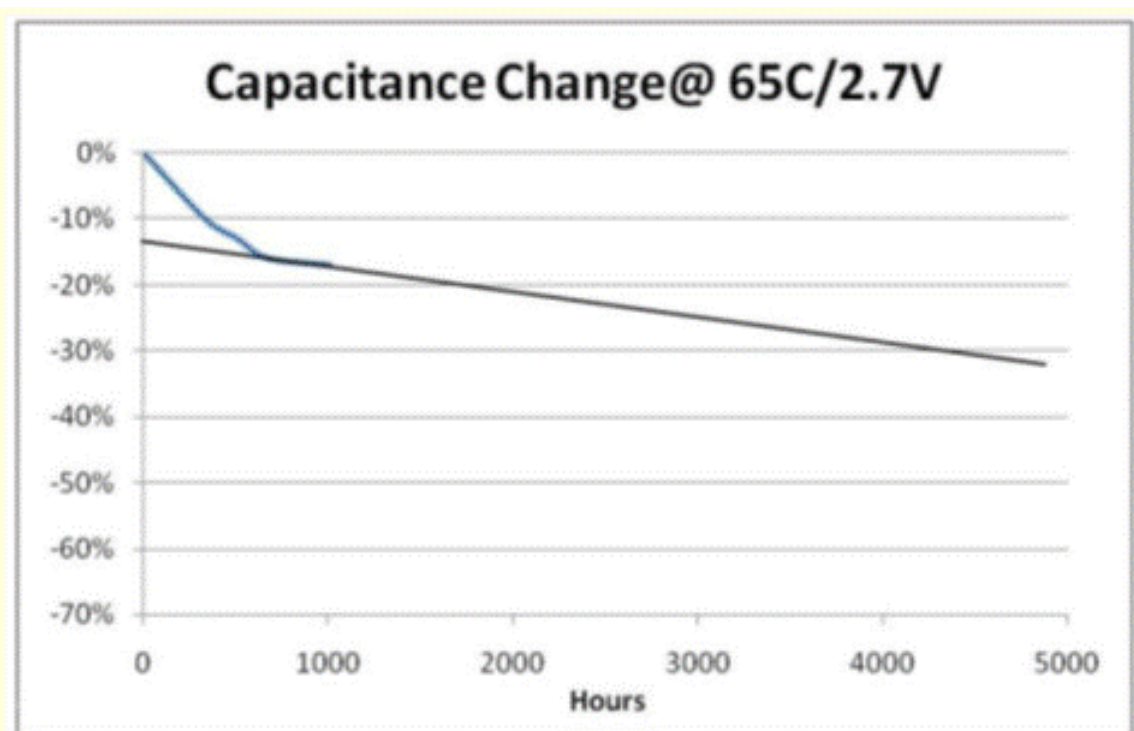
Failure under Abuse Conditions

Over voltage

- Loss of capacitance
- Increase of ESR
- Bulging
- Possible venting

Over temperature

- Loss of capacitance
- Increase in ESR
- Bulging
- Possible venting

Mechanical Stress

- Deformation
- Broken lead
- Increase in ESR

What Is The Self Discharge Or Leakage Current?

Self Discharge: Is the voltage drop on a charged cell after a set period of time without a load.

Leakage Current: Is the stable parasitic current expected when capacitor is held indefinitely on charge at the rated voltage. This value is voltage and temperature dependent.

Leakage Current TPL6.0/8X30F
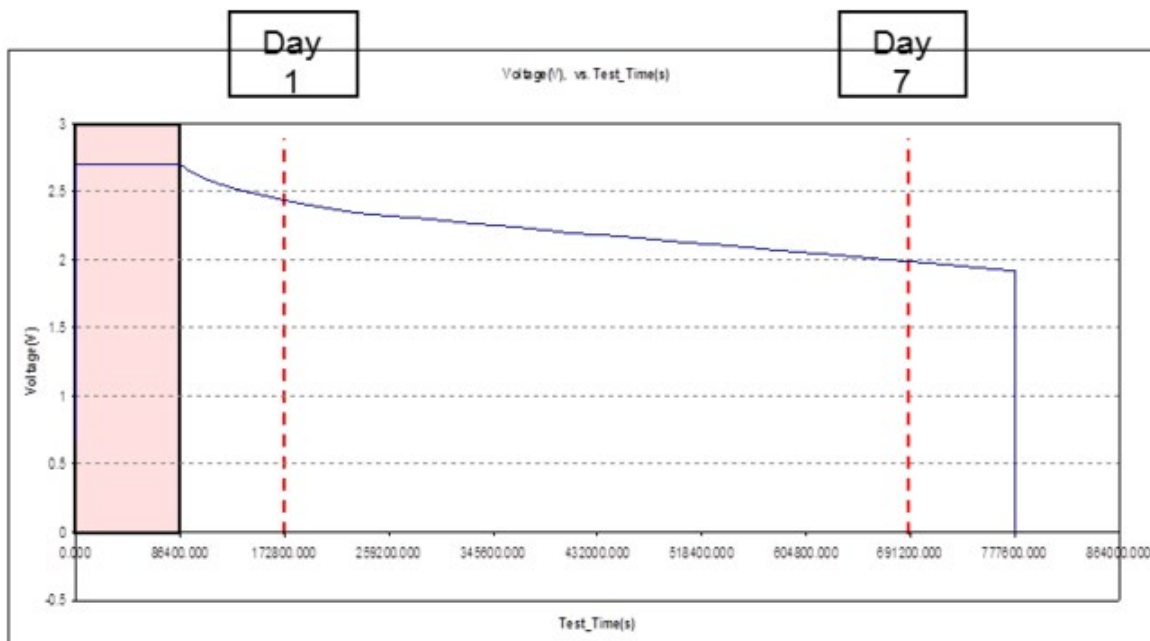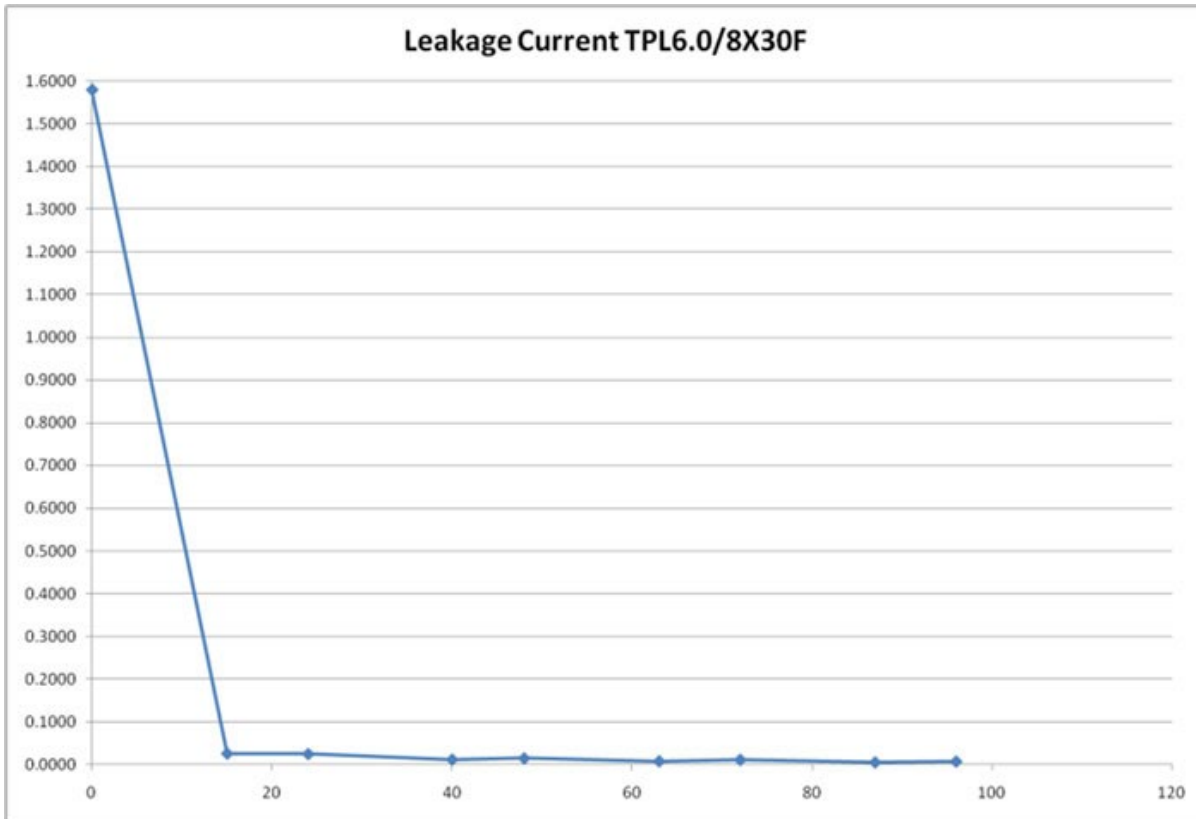
Series/Parallel Combination Of Ultracapacitors?

The voltage rating of PowerBurst® product is 2.7V per cell, which is mainly derived from the electrochemical stability of the electrolyte and electrode materials. The PowerBurst® family of products uses an organic electrolyte. The key advantage of an organic electrolyte versus other (i.e. aqueous) electrolytes is its higher voltage stability. In general, if cells are operated above their rated voltage for a long period of time, the life is reduced. This is a result of the electrolyte breakdown with exposure to high voltage. The amount of damage varies based on the voltage and the amount of time the cell is exposed to the over-voltage condition. Thus, occasional spikes above rated voltage will not immediately affect the capacitor.

Since in most applications the required voltage is above 2.7V multiple cells will need to be placed in series. Depending on the required energy there could be a need to then place multiple cells in parallel. When ultracapacitor cells are placed in series or parallel they react very similar to conventional capacitors. Below is a summary of key attributes when placing multiple cells in series/parallel formation:

Voltage

Series connection: When placing cells in series the overall voltage is increased directly by the number of cells in series.

Example: 4 cells (rated at 2.7V each) connected in series will have a maximum voltage of 10.8V.

Parallel connection: Placing cells in parallel will not affect the voltage.

Example: 4 cells (rated at 2.7V each) connected in parallel will have a maximum voltage of 2.7V.

Capacitance

Series connection: When placing same value cells in series the system capacitance is reduced by the number of cells placed in series based on the formula below:

$$Csys = \frac{Ccell}{n}$$

Example: 4 x 10F cells (rated at 2.7V each) connected in series will have a capacitance of 2.5F and a maximum voltage of 10.8V.

Parallel connection: Placing same value cells in parallel will increase the overall system capacitance proportionally to the number of cells placed in parallel:

$$Csys = Ccell * n$$

Example: 4 x 10F cells (rated at 2.7V each) connected in parallel will have a capacitance of 40F and a maximum voltage of 2.7V.

ESR

Series connection: By placing same value cells in series the overall system ESR will increase proportionally to the number of cells placed in series:

$$ESRsys = ESRcell * n$$

Example: 4 x 10F cells (DC ESR 75 mΩ each) connected in parallel will have a total ESR of 18.75 mΩ.

Leakage Current

Series connection: Placing same value cells in series will not affect the leakage current. The overall

leakage current will be the same as the single cell**.

Example: 4 x 10F cells (Leakage current of 0.03mA) connected in series will have a total leakage current of 0.03mA**.

Parallel connection: Placing cells in parallel will increase the overall leakage current proportionally to the number of cells placed in parallel**.

$$LCsys = LCcell * n$$

Example: 4 x 10F cells (Leakage current of 0.03mA) connected in parallel will have a total leakage current of 0.12mA**.

**It should be noted that this does not take into account leakage current induced as a result of cell balancing. In case of passive balancing the leakage current will be dominated by the bypass resistor value. For additional information on cell balancing refer to PowerBurst Product Guide under Design Consideration/Interconnection section.

Why Do Ultracapacitors Require Balancing? What Are The Balancing Methods?

For most applications a single cell at low voltage is not very useful and multiple cells are required to be placed in series. Since there is a tolerance difference between manufactured cells in capacitance, resistance and leakage current there will be an imbalance in the cell voltages of a series stack.
It is important to ensure that the individual voltages of any single cell do not exceed its maximum recommended working voltage as this could result in electrolyte decomposition, gas generation, ESR increase and ultimately reduced life.

This imbalance is initially dominated by the capacitance difference between the cells (i.e. a cell with a lower capacitance will charge to a higher voltage in a series string). For example, if two cells of 10F each are connected in series with one at +20% of nominal capacitance and the other at -10%, then the worst case voltage across the capacitors can be calculated by:

Vcap1=Vsupply x (Ccap1/(Ccap1 + Ccap2)

Assuming Vsupply=5.4V

Vcap1=5.4 x (12/(12+9)) = 3.08V

As can be seen, a proper cell balancing scheme needs to be placed within series connected cells to ensure no cell sees higher than rated voltage.
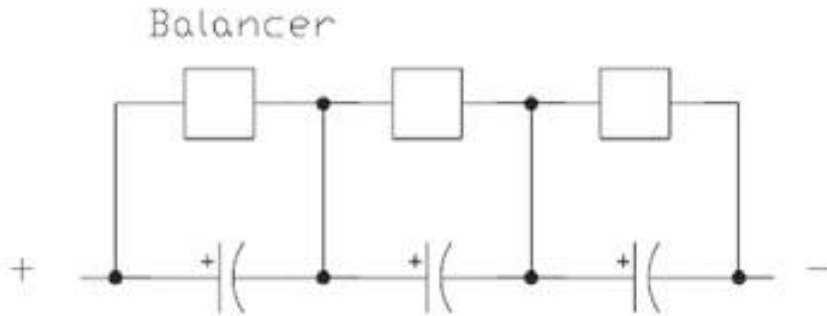
Also, when the cells are on charge for a period of time the leakage current will dominate this difference (i.e. a cell with a higher leakage current will go to a lower voltage distributing the voltage amongst other cells resulting in an over-voltage). Proper cell balancing can eliminate this imbalance. There are two balancing schemes to tackle this problem, and ensure a properly balanced module. They are:

Passive Balancing: One technique to compensate for variations in parallel resistance is to place a same valued bypass resistor in parallel with each cell, sized to dominate the total cell leakage current. This effectively reduces the variation of equivalent parallel resistance between the cells which is responsible for the leakage current. For example, if the cells have an average leakage current of 10uA +/- 3uA, a 1% resistor which will bypass 100uA may be a good choice. By using this resistor in parallel to each cell the average leakage current is now 110uA +/- 4uA. Introduction of this resistor has now decreased the variation in leakage current from 30% to 3.6%.
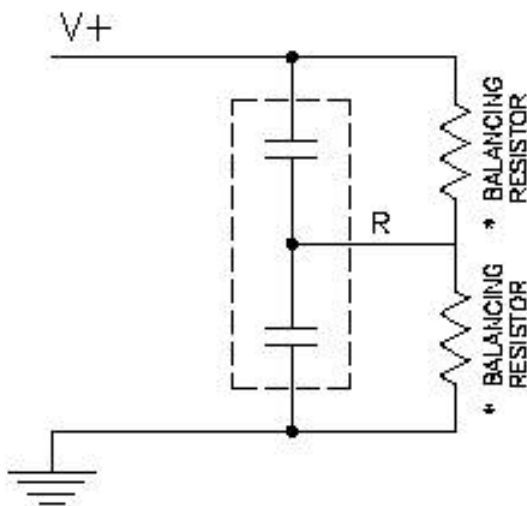

By having the same value resistor in parallel with all cells, the cells with higher voltages will discharge through the parallel resistor at a higher rate than the cells with lower voltages. This will help to distribute the total stack voltage evenly across the entire series of capacitors.

Passive voltage balancing is only recommended for applications that don't regularly charge and discharge the ultracapacitors and that can tolerate the additional load current of the balancing resistors. It is suggested that the balancing resistors be selected to give additional current flow of at least 10 times the worst-case cell leakage current. Higher ratio can be used to balance the cells

faster. A typical tradeoff is based on time to balance vs. leakage current. Once the system is balanced response time to balance is less of an issue unless a system it being severely cycled.

Active Balancing: For applications with a limited energy source or high level of cycling an active voltage balancing circuit is preferred since it typically draws much lower current in steady state and only requires larger currents when the cell voltage is out of balance. The active circuit forces the voltage at the nodes of series connected cells to stay below a fixed reference voltage.

In addition to ensuring accurate voltage balancing, active circuits typically draw much lower levels of current in steady state, and only require larger currents when the capacitor voltage goes out of balance. These characteristics make active voltage balancing circuits ideal for applications that charge and discharge the cells frequently as well as those with a finite energy source.
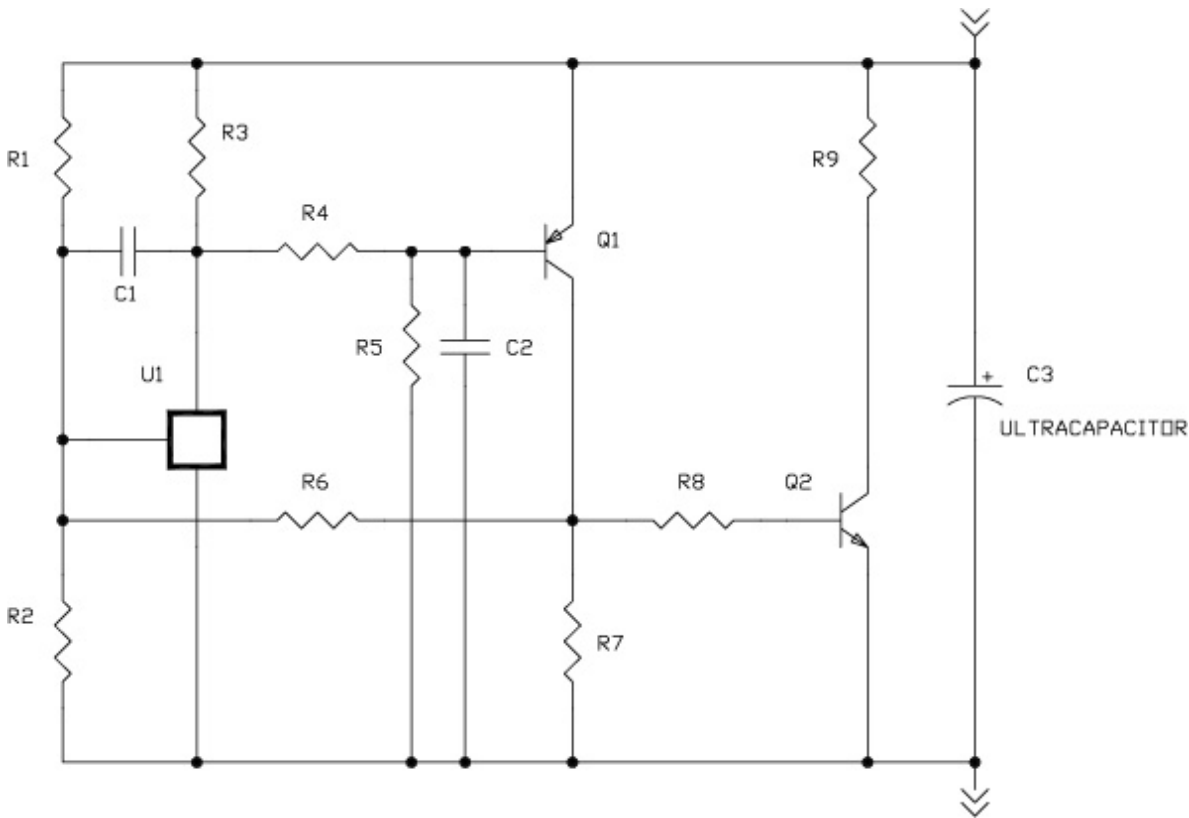
What Are The Temperature Effects On An Ultracapacitors?

One of the main advantages of ultracapacitors is its wide temperature range. The effect of temperature on ultracapacitor cells is two fold:

1. Life: Operating at high temperature extremes will reduce the life of the cells.
2. Performance: Operating at low temperature extremes will increase the internal resistance of the cell.

Cap / Esr change vs. Temperature
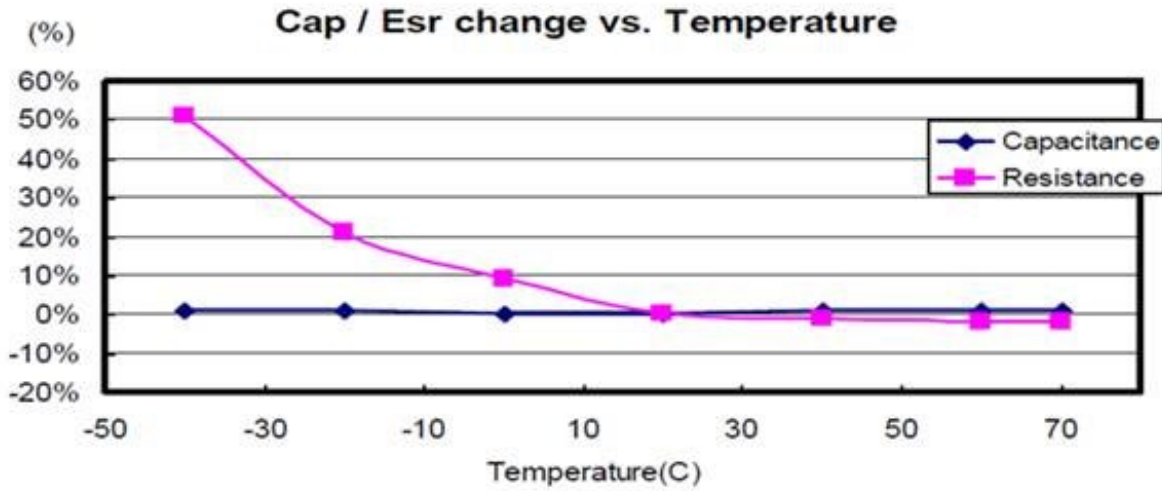
How To Measure An Ultracapacitor?

A constant current discharge test may be useful for customer evaluation of the product prior to application testing. All ultracapacitors are stored discharged for safety. We recommend completely discharging any capacitors that will not be installed into equipment.

Below is a list of equipment required to perform a typical constant current discharge test:

bi-directional power supply (supply/load) OR

separate power supply and programmable load (constant current capable)

voltage vs. time measurement and recording device (digital scope, or other data acquisition)

current vs. time measurement and recording device (optional if you can trust the power supply and load settings)

Before testing, connect data acquisition equipment to the device terminals, and set recording speeds as fast as reasonably possible (<<100msec preferred, the faster, the more accurate the calculations).

Setup

Set the power supply to the appropriate voltage and current limits, and turn the supply output OFF.

The current limit can be anything at or less than the maximum rated current for the cell. When performing repetitive high current testing, cooling air should be provided.

The voltage limit is the maximum cell voltage, times the number of cells in series. A single cell should be limited to 2.7 volts. Six cells in series (for example) can be operated at any voltage up to 16.2 volts (6 x 2.7V = 16.2V).

Connect the ultracapacitor to the power supply (having pre-set the current and voltage limits).

Cooling air may be required to keep the ultracapacitor within operating temperature limits, depending on the test current and duration.

Connect the voltage and current measuring/recording devices.

Charge

With the power supply pre-set, and the ultracapacitor connected, turn the supply output ON.

Charge the ultracapacitor at the appropriate current to the appropriate voltage.

Discharge

Note: If using a separate programmable load instead of an integrated bi-directional power supply, disconnect the charging power supply prior to discharging. (Don't simply turn it off or change its set points, as many supplies will sink current when not regulating.)

Set the load to the appropriate constant current, and discharge to 0.1V, or as low as the load can be controlled.

IMMEDIATELY remove the load once the minimum voltage is reached, allowing the device's voltage to "bounce" back.

(The discharge can actually be stopped at any voltage. Depending on equipment, some units can be discharged to 0.1V, and others discharged to ½ of the initial voltage. Values of capacitance will be slightly higher when discharged to ½ initial voltage rather than 0.1V.)

Measure the following parameters: (reference figure 1)
V_w = initial working voltage V_{min} = minimum voltage under load

I_d = discharge current V_f = voltage 5 seconds after removal of load.

t_d = time to discharge from initial voltage to minimum voltage

Capacitance calculation:

Capacitance = $(I_d * t_d)/(V_w - V_f) = (I_d * t_d)/V_d$

(This change in voltage ($V_w - V_f$) is used because it eliminates the voltage drop due to the equivalent series resistance)

Equivalent Series Resistance (at "DC") calculation:

ESR = $(V_f - V_{min})/I_d$

(An LCR meter or bridge can be used to measure ESR at higher frequencies. The ESR at frequencies up to 100Hz will typically be 50-60% of the "DC" ESR. The capacitance will be much lower, due to the structure of the electrode.)

(Note that calculations for Capacitance and Resistance can also be done on the charge)
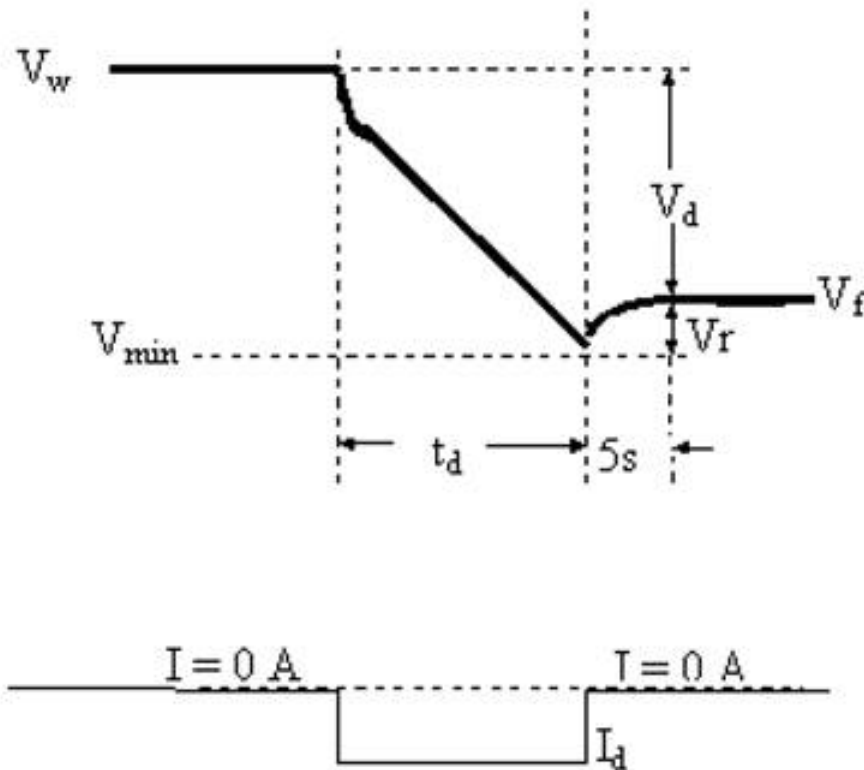
Constant Current Discharge Test

Figure 1: Representative measurement points for constant current test

Safety Considerations

As in all electrical testing, you as the investigator should take appropriate cautions in the design and execution of the test. Proper precautions for the appropriate voltage should be observed. Any interconnections should be sized for the maximum anticipated current, and insulated for the appropriate voltage. If repeated testing will be performed, cooling air may be required to keep the test unit within its operating temperature range.

How To Size An Ultracapacitor For Your Application?

Tecate Group offers a large selection of ultracapacitor cells and modules for various applications. In order to size the appropriate ultracapacitor cell for any application, we will need to determine the system variables needed. Using this information we can calculate the appropriate size and number of cells needed.

- In order to get a complete solution, the following parameters will need to be defined:
- Maximum Charged Voltage (Vmax), if different from Working Voltage then also (Vw)
- Minimum Voltage (Vmin)
- Required Power (W) or Current (I)
- Duration of Discharge (td)
- Duty Cycle
- Required Life
- Average Operating Temperature

The last three parameters are used to determine the life degradation factor to use. This is not discussed here but is a consideration to be taken by user. In order to know the appropriate size and also the number of cells required one needs to perform some simple sizing exercise. Most applications can be categorized into two categories: constant current applications or constant power applications. We will examine each one separately.

During the discharge cycle of an ultracapacitor there are two parameters to consider. The drop in voltage due to internal resistance, and the drop in voltage due to capacitance, as shown in Figure 1.
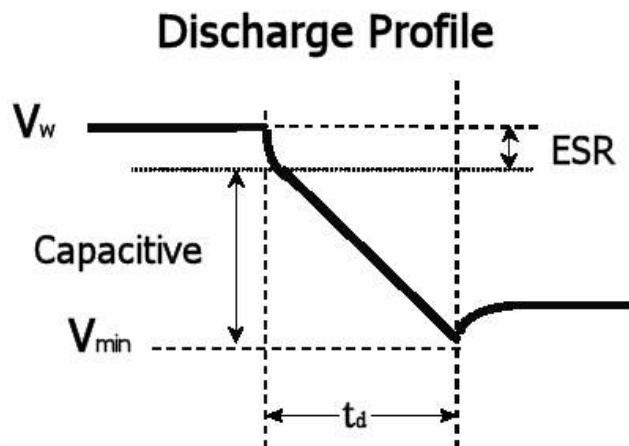

Figure 1: Discharge Curve

As can be seen above during a discharge cycle the initial drop in voltage is due to the Equivalent Series Resistance of the part (ESR). The amount of drop is a function of the ESR and discharge current as indicated by the equation below:

Equation 1

dVESR= I * ESR

After the initial instantaneous drop due to ESR, the capacitor will discharge according to its capacitance and discharge current as indicated in equation 2:

Equation 2

dVcap= I * td/C

By placing these two equations together the total voltage drop can be calculated per equation 3:

Equation 3

dVTotal = I *td/C + I * ESR

A brief overview of the variables in above equation:

dVTotal= The drop in voltage when the capacitor is discharged. This is the difference between the Vw and Vmin as

indicated on Figure 1. As can be seen in equation 3 this is the sum of the resistance and capacitance drop.

Note:

Allowing a larger dV will reduce the capacitance size used. Typically by allowing the capacitor to drop to ½ Vw,

75% of the capacitor energy is discharged.

I= Current in Amps used to discharge the capacitors. For equation 3 we assume this to be a constant current discharge.

td= Duration in Seconds to discharge the capacitor between Vw and Vmin.

C= the total capacitance of the ultracapacitor. If a single cell is used, then it is the cell capacitance. If multiple cells are used the equivalent capacitance is based on the number of capacitors in series or parallel. For capacitors in series the capacitance is additive at 1/C. For capacitors in parallel the capacitance is additive.

Equation 4

CTotal = Ccell * (# parallel/# series)

ESR= the total resistance of the ultracapacitor. If single cell is used then it is the cell resistance. If multiple cells are used the equivalent resistance is based on the number of capacitors in series or

parallel. For capacitors in series the resistance is additive. For capacitors in parallel the resistance is additive at 1/resistance.

Equation 5

ESRTotal=ESRcell * (#series/#parallel)

Constant Current Application

In the example below we will look at an application where the load requirement is a constant current.

Example 1:

Let's assume we have a requirement as follows:

Vmax= 15V

Vmin= 9V

I= 4 A

td= 5 sec

Using the information above we can use two methods to try and find the appropriate capacitor size.

Method 1:

We can ignore the ESR effect on the voltage drop to get an estimate on the capacitance and then resolve Equation 3 to see if the size picked is appropriate with the ESR effect, and if not, to increase to the next cell size.

So by taking out the ESR portion of equation 3 and solving for C we get:

Equation 6

C = I*td/dV Equation 6

By substituting the above parameters we get:

C = 4*5/ (15-9) = 3.33F

Note that this is the total capacitance at 15V. Since each ultracapacitor cell is typically rated at 2.7V, then we divide Vmax by 2.7 and round up:

15/2.7 = 5.5, so 6 cells in series.

Using equation 4 and assuming one parallel set then we estimate the cell needed will be in the range of:

Ccell= CTotal * # in series = 3.3 * 6 = 19.8F

Looking at the product offering we see the closest size is a 22F cell with an ESR value of 45 mohm. Taking the capacitance and ESR value of this cell we can plug it into equation 3 to see if the total voltage drop is within the application limit of 6V (note that we need to calculate the system C and ESR for 6 cells in series):

dVTotal= (4*5/ (22/6)) + (4* (.045*6)) = 5.46 + 1.08 = 6.54V

As can be seen the above voltage drop is more than the 6V allowed. Therefore we need to move to the next size up cell and redo the calculation. Also please note the values used are the initial specifications. To take into consideration end of life degradation one needs to apply the degradation factors to the capacitance and resistance numbers.

Method 2:

For the same parameters as above we can solve for the cell value using the RC time constant. The RC time constant of an ultracapacitor is the product of its capacitance value and resistance value. For the Tecate product TPL series we can use 0.8 seconds as an average.

Since R*C=0.8 seconds, then R=0.8/C

By substituting the above in equation 3 we get the following:

dVTotal= I*td/C + I*0.8/C

Solving for C, we get:

C = I/dVTotal*(td+0.8)

By substituting the value give (dV=6, I=4 and td=5) we solve the above equation for C:

C= 3.86F

Please note this is the stack capacitance and we need to solve for the cell capacitance. Based on the Vmax of 15V we determined we need 6 cells in series. So using equation 4 we solve for the cell capacitance as follows:

Ccell=CTotal* # series

Ccell= 3.86 * 6 = 23.16F

We will then use the data sheet to round this up to the closest cell available, which in this case is 25F.

Constant Power Application

In the example below we look at an application where the load is on a constant power discharge.

Example 2:

Let's assume we have a requirement as follow:

Vmax = 15V

Vmin = 9V

Power (P) = 60W

td = 5 sec

Using the information above we can use two methods to try and find the appropriate capacitor size.

Method 1:

A simple method will be to calculate an average current based on the above parameters and then apply the constant current sizing method to calculate the most appropriate cell:

Imax = Power/Vmin = 60/9 = 6.67 Amps

Imin = Power/Vmax = 60/15 = 4 Amps

Iavg = (6.67 + 4)/2 = 5.34 Amps

Using the method 1 sizing of the constant current application mentioned earlier we get a cell value of 26.7F. Rounding it up to the next cell value we find out the 30F cell is the appropriate cell for this application. Please note we typically recommend oversizing the cell by 20-30% to accommodate any degradation over time.

Method 2:

We can also calculate the appropriate cell size based on the energy needed. This method works well for low power application where the loss due to ESR is minimal.

Energy Needed = 60W * 5 sec = 300 Joules

The equation calculating the energy stored in a capacitor is:

Equation 8

E (joules) = 0.5 * C (V2max – V2min)

Substituting the values in equation 8 and solving for C we get:

$300 = 0.5 * C (225 - 81)$

$C = 4.17\ F$

Since we have 6 cells in series the cell capacitance needed is:

$4.17 * 6 = 25.02\ F$

Note that the above method did not take into account any losses due to ESR, thus resulting in a slightly smaller cell value.