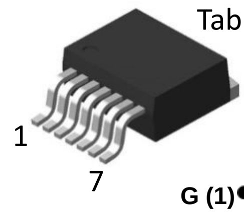
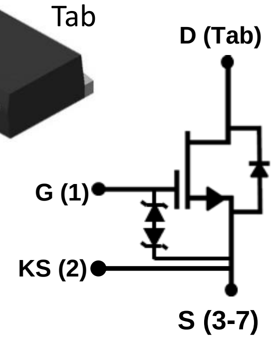
Description

United Silicon Carbide's cascode products co-package its high-performance G3 SiC JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits ultra-low gate charge, but also the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.





Part Number	Package	Marking
UF3C120150B7S	D2PAK-7L	UF3C120150B7S

Features

- Typical on-resistance $R_{DS(on),typ}$ of 150mΩ
- Maximum operating temperature of 175°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected, HBM class 2

Typical Applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C=25°C	18.4	A
		T_C=100°C	13.8	A
Pulsed drain current [2]	I_{DM}	T_C=25°C	38	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =2A	30	mJ
Power dissipation	P_{tot}	T_C=25°C	166.7	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8” from case for 5 seconds	T_L		250	°C

1 Limited by $T_{J,max}$

2 Pulse width t_p limited by $T_{J,max}$

3 Starting T_J = 25°C

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	1200			V
Total drain leakage current	I_{DSS}	V_{DS}=1200V, V_{GS}=0V, T_J=25°C		0.4	50	µA
		V_{DS}=1200V, V_{GS}=0V, T_J=175°C		6		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		6	±20	µA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=5A, T_J=25°C		150	180	mΩ
		V_{GS}=12V, I_D=5A, T_J=175°C		330		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=10mA	3.5	4.4	5.5	V
Gate resistance	R_G	f=1MHz, open drain		4.6		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C=25°C			18.4	A
Diode pulse current [2]	$I_{S,pulse}$	T_C=25°C			38	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_F=5A, T_J=25°C		1.46	2	V
		V_{GS}=0V, I_F=5A, T_J=175°C		2		
Reverse recovery charge	Q_{rr}	V_R=800V, I_F=13A, V_{GS}=-5V, R_{G_EXT}=20Ω di/dt=1400A/µs, T_J=25°C		73		nC
Reverse recovery time	t_{rr}			20		ns
Reverse recovery charge	Q_{rr}	V_R=800V, I_F=13A, V_{GS}=-5V, R_{G_EXT}=20Ω di/dt=1400A/µs, T_J=150°C		70		nC
Reverse recovery time	t_{rr}			18		ns

Typical Performance - Dynamic

Parameter	symbol	Test Conditions	Value Min	Value Typ	Value Max	Units
Input capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V, f=100kHz		731		pF
Output capacitance	C_{oss}			56		
Reverse transfer capacitance	C_{rss}			1		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 800V, V_{GS}=0V		32		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 800V, V_{GS}=0V		67		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=800V, V_{GS}=0V		10.2		μJ
Total gate charge	Q_G	V_{DS}=800V, I_D=13A, V_{GS}=-5V to 15V		27.5		nC
Gate-drain charge	Q_{GD}			5		
Gate-source charge	Q_{GS}			11		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=13A, Gate Driver =-5V to +12V, Turn-on $R_{G,EXT}$=8.5Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: same device with V_{GS} = -5V, R_G = 20Ω T_J=25°C		29		ns
Rise time	t_r			7		
Turn-off delay time	$t_{d(off)}$			26		
Fall time	t_f			6		
Turn-on energy	E_{ON}			212		μJ
Turn-off energy	E_{OFF}			49		
Total switching energy	E_{TOTAL}			261		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=13A, Gate Driver =-5V to +12V, Turn-on $R_{G,EXT}$=8.5Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: same device with V_{GS} = -5V, R_G = 20Ω T_J=150°C		26		ns
Rise time	t_r			6		
Turn-off delay time	$t_{d(off)}$			27		
Fall time	t_f			6		
Turn-on energy	E_{ON}			187		μJ
Turn-off energy	E_{OFF}			49		
Total switching energy	E_{TOTAL}			236		

Thermal Characteristics

Parameter	symbol	Test Conditions	Value Min	Value Typ	Value Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.7	0.9	°C/W

Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (Coss), gate charge (Qg), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see www.unitedsic.com.

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