APPLICATION NOTE

GaN Bias Circuit Design Guidelines

Introduction

This document provides general bias circuit design information for GaN transistors. There are many different design approaches that can be used to successfully implement GaN bias circuits where tradeoffs can be made to optimize performance, cost, size, and complexity for the application. This document highlights minimal bias circuit design requirements to prevent unintended bias conditions that can affect performance or lead to device failure. For assistance with bias circuit design contact Qorvo applications support.

Referenced Material

“How to Bias GaN Transistors: An Introduction Tutorial,” Qorvo® Instructional Video for more Qorvo GaN bias information

https://www.qorvo.com/design-hub/videos/how-to-bias-gan-transistors-an-introduction-tutorial

Bias Sequencing

Qorvo GaN devices are depletion mode devices and therefore require a negative gate voltage while the drain voltage is present to prevent damage. With the gate at V_{GS} = 0 V and with drain voltage present a device will have high current and high-power dissipation which can permanently damage a device. The user should insure via hardware or software control that negative gate voltage is always present on the device whenever there is drain voltage present. The user should also account for discharge of bypass capacitors on the drain bias feeds which can hold voltage for a time period after the drain power supply voltage is removed.

An example bias sequence for biasing from a data sheet is shown in Table 1.

Bias-up Procedure	Bias-down Procedure
1. Set V_G to -4 V.	1. Turn off RF signal.
2. Set ID current limit to 100 mA.	1. Turn off VD
2. Apply 50 V VD.	3. Wait 2 seconds to allow drain capacitor to discharge
4. Slowly adjust VG until ID is set to 50 mA.	4. Turn off VG
5. Set ID current limit to 1.5 A	
6. Apply RF.	

Table 1 Qorvo QPD1004 Bias Sequence

Setting Bias Current

The user sets the I_{DQ} bias current of the device by adjusting the gate voltage (V_{GS}). Due to threshold variation of GaN devices, Qorvo recommends adjusting the gate voltage for every device to maintain consistent quiescent bias current from part to part. A fixed gate voltage bias circuit will lead to a wide range of I_{DQ} due to threshold variation. The fixed voltage case can range from low or no current at I_{DQ} to very high I_{DQ} current across the distribution of devices. Low I_{DQ} can affect RF performance and the high current can also affect performance and even damage the device if the current is too high.

The designer can consult the data sheet for reference bias conditions. The designer also has flexibility to adjust the bias differently than the data sheet to optimize for different performance criteria. Adjusting the quiescent current impacts gain, efficiency, linearity, and stability. The bias can be optimized to trade-off between these parameters. When deviating from the recommended data sheet bias conditions the designer needs to verify that dissipated power limits or supply voltage limits are not exceeded.

Temperature affects the threshold voltage which will lead to variation in drain current with a constant gate voltage. An example of I_{DQ} versus temperature with a fixed V_{GS} is shown in Figure 1. If the application requires maintaining constant current over temperature as is required in linear applications V_{GS} must be adjusted in order to maintain constant current. An example of V_{GS} to maintain a fixed I_{DQ} is shown in Figure 2.

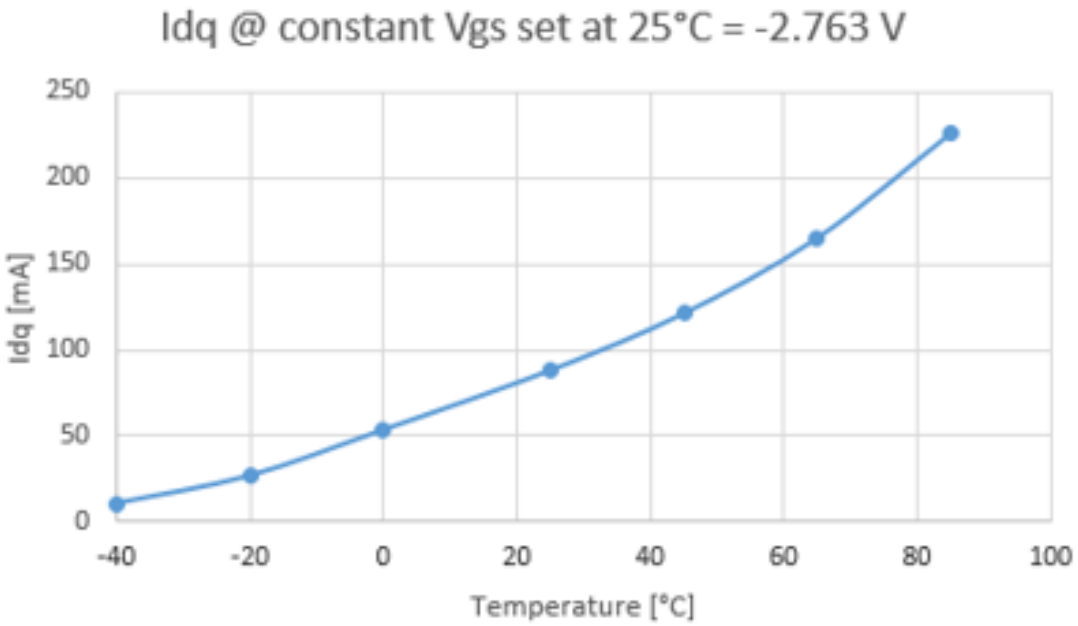

Figure 1. I_{DQ} versus temperature with a fixed V_{GS}

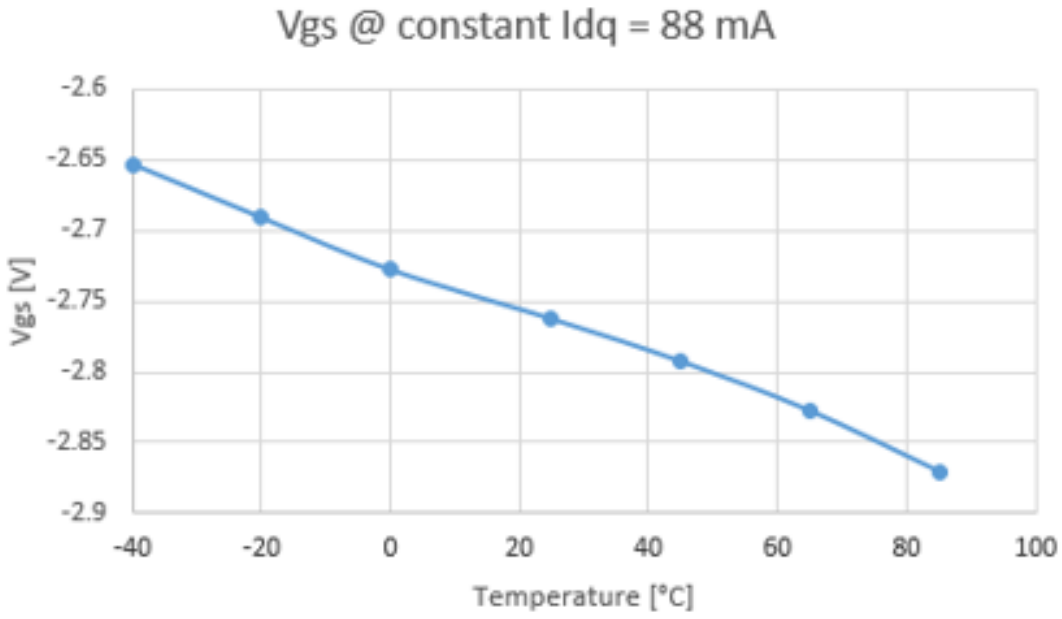

Figure 2. V_{GS} versus temperature to maintain constant I_{DQ}

Bias Bypass Network Design

GaN bias network design requires attention to several aspects in order to ensure that the devices can be operated correctly and not inadvertently damaged. The bias networks that connect power supplies to RF or millimeter wave products must be properly decoupled. Use of bypass capacitors not only filters unwanted ripple and noise in the supply, but also serve as charge sources for the device. Bypass capacitors help negate the lead inductance in power supply lines. Stability also needs to be considered when designing bypass networks. The bias networks will interact with the device and the combined response will influence stability. The frequency response of the bypass capacitors can influence performance and stability, so designers will sometimes dampen the response by including resistors in series to de-Q the capacitor's frequency response.

A series gate resistance is needed for all discrete FET-based GaN power amplifiers typically in the range of five to ten ohms minimum for stable operation. Adding the series resistance can have also have negative effects to the response so series resistance should be kept low. An example bias bypass network design is shown in the schematic in Figure 3. GaN MMIC power amplifiers usually have this series resistance designed in and integrated on chip, so the series resistance is usually not needed.

Recommended bypassing components and device layout are provided in the data sheet for each GaN device. The quantity, values, and locations of the bypass components have been demonstrated by Qorvo engineers during the development of the amplifier. Other bias bypass network implementations are possible, depending on the desired performance and environmental conditions. For alternate topologies and/or components, due diligence should be taken to make sure the device performs as desired (e.g. RF performance, linearity, device thermal behavior, stability, etc.) under all expected operating and environmental conditions.

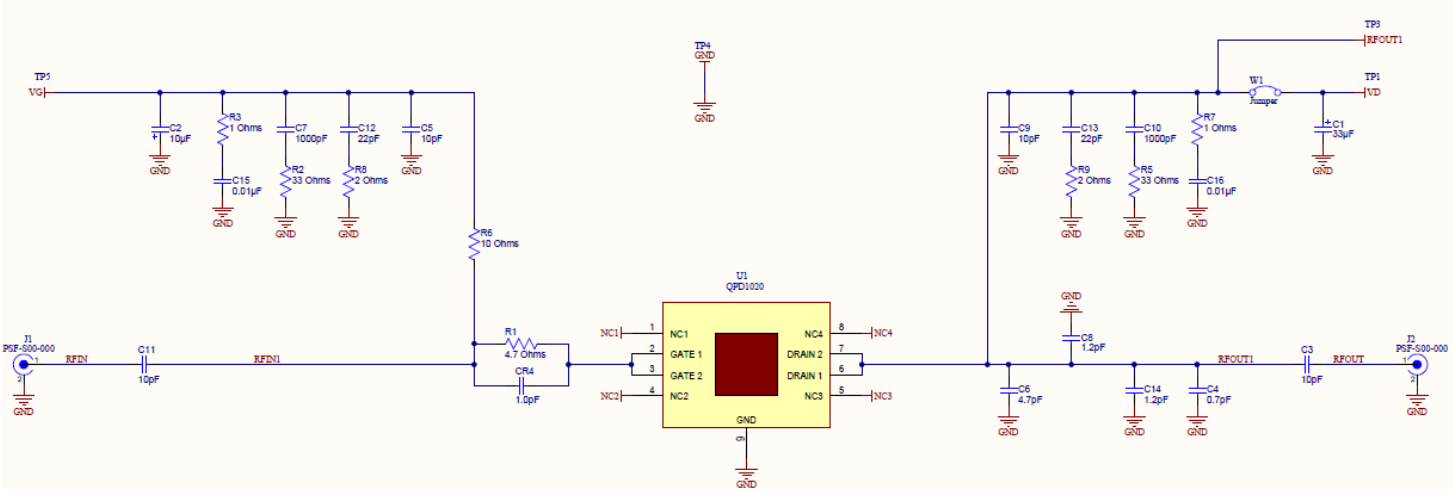

Figure 3. QPD1020 2.7-3.1GHz Application Schematic showing Gate (V_G and V_D) bypass networks

Design for Gate Current

The power supply and bias circuit need to be designed to be compatible with gate current. The bias circuitry needs to be able to sink and source current at the gate. Gate leakage current flows out of the device and into the bias circuitry. At high drive levels gate current will flow into the device due to rectification of RF drive by the gate diode. The amount of gate leakage current is related to the size of the device. A higher power, larger transistor will have higher gate leakage current compared to a smaller device. Testing leakage of a small population of parts is not enough to use as a guideline for the limit of leakage. Instead, the data sheet should be consulted, or an application engineer should be contacted to account for the gate leakage limit in the bias circuit design.

If there is large equivalent series resistance between the bias circuitry and the GaN device the gate leakage current will cause a voltage drop across the resistor which will alter the bias voltage. If this drop is large enough, the device will have high I_{DQ} and can even be damaged due to high dissipation. Gate leakage current limits are in the range of milliamps (mA). As an example, if a device has -1mA of leakage current and 1 kΩ series resistance there will be 1 V drop across the series resistor. This can have serious consequences when setting the bias if the expected Vg is 1V more positive then the intended setting. Thus, low gate series resistance should be selected. Ideally, series gate resistance in the gate bias network should be high enough for RF stability of the GaN transistor with margin, but still low enough not to alter the intended bias set point. The stability of the active bias network components also needs to be considered as part of the design. The active bias circuitry may require specific loading to stay stable therefore the bias network and GaN device stability need to be designed in conjunction.

Forward gate current, which occurs at high drive levels, also needs to be considered in the design. The active bias circuitry needs to be able to support the RMS forward current. Bypassing capacitors can be used to source the gate current during peak drive conditions for pulsed or modulated applications. Gate current increases as input power is increased. Worst case forward bias current occurs at cold temperatures. The coldest application temperature and highest drive level should be considered to determine the forward current capacity needed in the active bias circuit design.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

Contact Information

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